# CTT Series - Digital Counter / Timer / Tachometer

## Timer Mode

### Timer Performance Specifications

<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of Digits</td>
<td>6 digits on each line</td>
</tr>
<tr>
<td>Display</td>
<td>Present values: red LED, character height 8mm; Set value: green LED, character height: 6mm</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Setting</th>
<th>Range</th>
<th>Units</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>sec</td>
<td>0.01 – 9,999.99</td>
<td>A unit = 10ms</td>
<td>9,999.99 secs.</td>
</tr>
<tr>
<td>sec</td>
<td>0.1 – 99,999.9</td>
<td>A unit = 0.1 sec.</td>
<td>99,999.9 secs.</td>
</tr>
<tr>
<td>sec</td>
<td>1 – 999,999</td>
<td>A unit = 1 sec.</td>
<td>999,999 secs.</td>
</tr>
<tr>
<td>min., sec.</td>
<td>0.01 – 9,995.99</td>
<td>A unit = 0.01 sec.</td>
<td>9,995.99 secs.</td>
</tr>
<tr>
<td>min., sec.</td>
<td>0.1 – 99,995.99</td>
<td>A unit = 0.1 sec.</td>
<td>99,995.99 secs.</td>
</tr>
<tr>
<td>min.</td>
<td>0.1 – 999,999</td>
<td>A unit = 0.1 min.</td>
<td>999,999 mins.</td>
</tr>
<tr>
<td>min.</td>
<td>1 – 999,999</td>
<td>A unit = 1 min.</td>
<td>999,999 mins.</td>
</tr>
<tr>
<td>hr., min., sec.</td>
<td>1 – 995,995</td>
<td>A unit = 1 sec.</td>
<td>995,995 secs. (100 hrs.)</td>
</tr>
<tr>
<td>hr., min.</td>
<td>1 – 999,995</td>
<td>A unit = 1 min.</td>
<td>999,995 secs. (10,000 hrs.)</td>
</tr>
<tr>
<td>hr.</td>
<td>1 – 999,999</td>
<td>A unit = 1 hr.</td>
<td>999,999 hrs.</td>
</tr>
</tbody>
</table>

## Timing Charts

### Signal On Delay 1

With power applied to the CTT, the leading edge of the input signal at START will begin the timing period setting value SV (timing up or down based on parameter [t modE] or by DIP switch 2). At the end of the timing period both outputs will turn ON momentarily for the time set in the output pulse width parameter ([tou1]) or will be maintained ON if the output pulse width parameter ([tou1]) is set to 0.00. The trailing edge of the “start” signal has no effect on the outputs or timing period.

The leading edge of a “reset” input signal at RST1 will turn OFF the outputs and reset the timing period. The “reset” signal minimum pulse width is set by reset pulse width parameter ([rtSr]) or DIP Switch 8.

The leading edge of a “pause” input signal at GATE will pause the timing period after it has been started. The timing period will continue after the trailing edge of the external switch “pause” (Gate) signal.

When power is removed, both outputs will turn OFF and the timing period will be reset.
Signal On Delay 2

With power applied to the CTT, the leading edge of the input signal at START will begin the timing period setting value SV (timing up or down based on parameter (Son) or by DIP switch 2). At the end of the timing period both outputs will turn ON momentarily for the time set in the output pulse width parameter (Soffd) or will be maintained ON if the output pulse width parameter (Soffd) is set to 0.00. The trailing edge of the “start” signal will turn OFF the outputs and reset the timing period.

The leading edge of a “reset” input signal at RST1 will turn OFF the outputs and reset the timing period. The “reset” signal minimum pulse width is set by reset pulse width parameter (rtSr) or DIP Switch 8.

The leading edge of a “pause” input signal at GATE will pause the timing period after it has been started. The timing period will continue after the trailing edge of the external switch “pause” (Gate) signal.

When power is removed, both outputs will turn OFF and the timing period will be reset.

Signal Off Delay

With power applied to the CTT, the leading edge of the input signal at START will immediately turn ON the outputs. The trailing edge of the “start” signal will begin the timing period setting value SV (timing up or down based on parameter (Son) or by DIP switch 2). At the end of the timing period both outputs will turn OFF. The leading edge of a “start” signal applied during a previously initiated timing period will reset the timing period.

The leading edge of a “reset” input signal at RST1 will turn OFF the outputs and reset the timing period. The “reset” signal minimum pulse width is set by reset pulse width parameter (rtSr) or DIP Switch 8.

The leading edge of a “pause” input signal at GATE will pause the timing period after it has been started. The timing period will continue after the trailing edge of the external switch “pause” (Gate) signal.

When power is removed, both outputs will turn OFF and the timing period will be reset.

Signal On

With power applied to the CTT, the leading edge of the input signal at START will immediately turn ON the outputs and begin the timing period setting value SV (timing up or down based on parameter (Son) or by DIP switch 2). The trailing edge of the “start” signal has no effect on the outputs or timing period. At the end of the timing period both outputs will turn OFF and the timing period will reset. The leading edge of a “start” signal applied during a previously initiated timing period will not reset the timing period.

The leading edge of a “reset” input signal at RST1 will turn OFF the outputs and reset the timing period. The “reset” signal minimum pulse width is set by reset pulse width parameter (rtSr) or DIP Switch 8.

The leading edge of a “pause” input signal at GATE will pause the timing period after it has been started. The timing period will continue after the trailing edge of the external switch “pause” (Gate) signal.

When power is removed, both outputs will turn OFF and the timing period will be reset.
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Power On Delay (Pond)

When power is applied to the CTT, the timing period setting value SV will begin (timing up or down based on parameter t modE). At the end of the timing period both outputs will turn ON momentarily for the time set in the output pulse width parameter tout1 or will be maintained ON if the output pulse width parameter tout1 is set to 0.00.

The leading edge of a “reset” input signal at RST1 will turn OFF the outputs and reset the timing period. The “reset” signal minimum pulse width is set by reset pulse width parameter rtSr.

The leading edge of a “pause” input signal at GATE or signal at START will pause the timing period after it has been started. The timing period will continue after the trailing edge of the external switch “pause” (Gate) or “start” signal.

When power is removed, both outputs will turn OFF and the timing period will be reset.

Power On Delay HOLD (PondH)

When power is applied to the CTT, the timing period setting value SV will begin (timing up or down based on parameter t modE). At the end of the timing period both outputs will turn ON momentarily for the time set in the output pulse width parameter tout1 or will be maintained ON if the output pulse width parameter tout1 is set to 0.00.

The leading edge of a “reset” input signal at RST1 will turn OFF the outputs and reset the timing period. The “reset” signal minimum pulse width is set by reset pulse width parameter rtSr.

The leading edge of a “pause” input signal at GATE or signal at START will pause the timing period after it has been started. The timing period will continue after the trailing edge of the “pause” (Gate) or “start” signal.

When power is removed, both outputs will turn OFF. The last state of the outputs and the last value of the current timing period will be “stored” in eeprom when power is removed. When power is reapplied the outputs will return to their last state and timing will resume from the last value of the timing period.
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Repeat Cycle (rCy)

With power applied to the CTT, the leading edge of the input signal at START will begin the timing period setting value SV (timing up or down based on parameter (t modE)). At the end of the timing period, the timing period will reset and repeat automatically.

If the output pulse width parameter (tOUT1) is set to 0.00 both outputs will turn ON at the end of the first timing period, turn OFF at the end of the next timing period, turn ON at the end of the next timing period, etc.

If the output pulse width parameter (tOUT1) is set to >0.00 both outputs will turn ON momentarily for the time set in the output pulse width parameter (tOUT1) at the beginning of each timing period.

The trailing edge of the “start” signal has no effect on the outputs or timing period.

The leading edge of a “reset” input signal at RST1 will turn OFF the outputs and reset the timing period. The “reset” signal minimum pulse width is set by reset pulse width parameter (rtSr). The leading edge of a new “start” signal is necessary to restart the cycle.

The leading edge of a “pause” input signal at GATE will pause the timing period after it has been started. The timing period will continue after the trailing edge of the external switch “pause” (Gate) signal.

When power is removed, both outputs will turn OFF and the timing period will be reset.

Repeat Cycle HOLD (rCyH)

With power applied to the CTT, the leading edge of the input signal at START will begin the timing period setting value SV (timing up or down based on parameter (t modE)). At the end of the timing period, the timing period will reset and repeat automatically.

If the output pulse width parameter (tOUT1) is set to 0, both outputs will turn ON at the end of the first timing period, turn OFF at the end of the next timing period, turn ON at the end of the next timing period, etc.

If the output pulse width parameter (tOUT1) is set to >0.00, both outputs will turn ON momentarily for the time set in the output pulse width parameter (tOUT1) at the beginning of each timing period.

The trailing edge of the “start” signal has no effect on the outputs or timing period.

The leading edge of a “reset” input signal at RST1 will turn OFF the outputs and reset the timing period. The “reset” signal minimum pulse width is set by reset pulse width parameter (rtSr). The leading edge of a new “start” signal is necessary to restart the cycle.

The leading edge of a “pause” input signal at GATE will pause the timing period after it has been started. The timing period will continue after the trailing edge of the external switch “pause” (Gate) signal.

When power is removed, both outputs will turn OFF. The last state of the outputs and the last value of the current timing period will be “stored” in Eeprom when power is removed. When power is reapplied the outputs will return to their last state and timing will resume from the last value of the timing period by the leading edge of a new “start” signal.
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Repeat Cycle 2 (rCy2)

With power applied to the CTT, the leading edge of the input signal at START will begin the timing period timing up or down based on parameter (t mode). At the end of the timing period, the timing period will reset and repeat automatically.

Both outputs will turn ON at the beginning of the first timing period and turn OFF when the timing period reaches time period setting SV2. The outputs will turn ON again when the time period reaches time period setting SV1.

The trailing edge of the “start” signal has no effect on the outputs or timing period.

The leading edge of a “reset” input signal at RST1 will turn OFF the outputs and reset the timing period. The “reset” signal minimum pulse width is set by reset pulse width parameter (rtSr0).

The leading edge of a “pause” input signal at GATE will pause the timing period after it has been started. The timing period will continue after the trailing edge of the external switch “pause” (Gate) signal.

When power is removed, both outputs will turn OFF and the timing period will be reset.

Signal Cumulate (Sc on)

With power applied to the CTT, the leading edge of the input signal at START will begin the timing period setting value SV timing up or down based on parameter (t mode). The trailing edge of the “start” signal will pause the timing period. The leading edge of a subsequent “start” signal will resume timing from the last value of the timing period. At the end of the timing period both outputs will turn ON.

The leading edge of a “reset” input signal at RST1 will turn OFF the outputs and reset the timing period. The “reset” signal minimum pulse width is set by reset pulse width parameter (rtSr0).

The leading edge of a “pause” input signal at GATE will pause the timing period after it has been started. The timing period will continue after the trailing edge of the external switch “pause” (Gate) signal.

When power is removed, both outputs will turn OFF. The last state of the outputs and the last value of the current timing period will be “stored” when power is removed. When power is reapplied the outputs will return to their last state and timing will resume from the last value of the timing period by the leading edge of a new “start” signal.
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Signal Twin ON-Start (St-on)

With power applied to the CTT, the leading edge of the input signal at START will turn ON the outputs and begin the timing period timing up or down based on parameter \( t \text{modE} \). When the timing period reaches time setting SV2 the outputs will turn OFF and the time period will reset and restart automatically. When the time period now reaches time setting SV1 the outputs will turn ON again and the time period will reset and repeat automatically.

The trailing edge of the “start” signal has no effect on the outputs or timing period.

The leading edge of a “reset” input signal at RST1 will turn OFF the outputs and reset the timing period. The “reset” signal minimum pulse width is set by reset pulse width parameter \( r \text{Sr} \). The leading edge of a new “start” signal is necessary to restart the cycle.

The leading edge of a “pause” input signal at GATE will pause the timing period after it has been started. The timing period will continue after the trailing edge of the external switch “pause” (Gate) signal.

When power is removed, both outputs will turn OFF and the timing period will be reset.

Signal Twin OFF-Start (St-off)

With power applied to the CTT, the leading edge of an input signal at START will begin the timing period timing up or down based on parameter \( t \text{modE} \). When the timing period reaches time setting SV1 the outputs will turn ON and the time period will reset and restart automatically. When the time period now reaches time setting SV2 the outputs will turn OFF again and the time period will reset and repeat automatically.

The trailing edge of the “start” signal has no effect on the outputs or timing period.

The leading edge of a “reset” input signal at RST1 will turn OFF the outputs and reset the timing period. The “reset” signal minimum pulse width is set by reset pulse width parameter \( r \text{Sr} \). The leading edge of a new “start” signal is necessary to restart the cycle.

The leading edge of a “pause” input signal at GATE will pause the timing period after it has been started. The timing period will continue after the trailing edge of the external switch “pause” (Gate) signal.

When power is removed, both outputs will turn OFF and the timing period will be reset.
CTT Series - Digital Counter / Timer / Tachometer

Features

• Can operate as a digital counter, timer, combination timer + counter or tachometer
• Accepts voltage and non-voltage inputs from a wide variety of NPN, PNP, or dry contact sensors
• Selectable counting speeds from 1 to 10,000 cycles per second
• Multiple transistor and relay outputs can operate as momentary or maintained
• Double-line, 6-digit, 2-color LCD display
• Easy configuration with externally accessible DIP switches or the lockable keypad
• Display decimal point selection
• Available in 100-240VAC and 24VDC powered models
• UL508 listed (E311366), cULus, CE marked

A lot of functionality in one powerful little unit!

The CTT series is an extremely versatile multi-function device that is easily configured for operation as a digital counter, timer, combination timer + counter, or tachometer. Both voltage and non-voltage inputs are accepted from a wide variety of sensor types with NPN, PNP, or dry contact outputs. The first output on the CTT is a single-pole, single-throw relay and NPN transistor that operate concurrently. The second CTT output can be ordered as either a single-pole, double throw relay or NPN transistor. Parameters are easily set using the externally accessible DIP switches or the lockable keypad. The double-line, 6-digit, two-color LCD display shows the counter, timer, or tachometer present values, setting values and menu parameters during set-up. Additional individual indicators are provided for inputs, outputs and functions. The standard 1/16 DIN size, with included panel mounting clip and gasket, make panel mounting a snap. The CTT is available in 100-240VAC and 24VDC powered models.

Visit www.automationdirect.com to download the free comprehensive CTT Series manual.

Click on the above thumbnail or go to https://www.automationdirect.com/VID-RL-0001 for a short introductory video for the CTT units.

For a full set of Demo and Set Up videos for the CTT units please scan the QR code or follow the link below. https://www.automationdirect.com/videos/home?link=link&cat1=60

For latest prices, please check AutomationDirect.com
CTT Series - Digital Counter / Timer / Tachometer

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CTT-AN-D24</td>
<td>Counter / Timer / Tachometer, Output 1 NPN &amp; SPST relay, Output 2 NPN, 24 VDC powered, panel mounting clip is included*</td>
</tr>
<tr>
<td>CTT-AN-A120</td>
<td>Counter / Timer / Tachometer, Output 1 NPN &amp; SPST relay, Output 2 NPN, 100-264 VAC powered, panel mounting clip is included*</td>
</tr>
<tr>
<td>CTT-1C-D24</td>
<td>Counter / Timer / Tachometer, Output 1 NPN &amp; SPST relay, Output 2 SPDT relay, 24 VDC powered, panel mounting clip is included*</td>
</tr>
<tr>
<td>CTT-1C-A120</td>
<td>Counter / Timer / Tachometer, Output 1 NPN &amp; SPST relay, Output 2 SPDT relay, 100-264 VAC powered, panel mounting clip is included*</td>
</tr>
</tbody>
</table>

* Spare panel clips part number PANEL-16

Digital Counter / Timer / Tachometer General Specifications

- **Input Power Requirements**: 100 to 240 VAC 50/60 Hz, 24 VDC
- **Operation Voltage Range**: 85 to 264 VAC, 21.6 to 26.4 VDC
- **Power Consumption**: Less than 10VA
- **Power Source**: 12VDC ±10%, 100mA
- **Display**: Double-line, 6-digit LCD display (SV = 8mm, PV = 6mm)
- **Input Signal**: NPN ON impedance: 1K ohm max. ON residual voltage: 2V max. PNP 4.5 to 30VDC, low level: 0 to 2VDC
- **Output 1**: Relay: SPST max. 250VAC, 5A (resistive load), 4A (inductive load); Transistor: NPN open collector. When 100mA @ 30VDC, residual voltage = 1.5VDC max
- **Output 2**: CTT-1C-xxx Relay: SPDT max. 250VAC/30VDC, 5A (resistive load), 4A (inductive load) CTT-AN-xxx Transistor: NPN open collector. When 100mA @ 30VDC residual voltage = 1.5VDC max
- **Life Expectancy**: Mechanical 10,000,000 operations (frequency 18,000 operations/hr) Electrical 100,000 operations (frequency 900 operations/hr)
- **Output Duration (where used)**: 0.00 (latching) / 0.01 to 99.99 seconds
- **Output Switching Time**: 2 milliseconds max
- **Dielectric Strength**: 2000VAC 50/60 Hz for 1 minute
- **Vibration Resistance**: Without damage: 10 – 55 Hz, amplitude = 0.75 mm, 3 axes for 2 hours
- **Shock Resistance**: Without damage: drop 4 times, 300m/s² 3 edges, 6 surfaces and 1 corner
- **ambient temperature**: +32°F to +122°F (0°C to +50°C)
- **Storage Temperature**: -4°F to +149°F (-20°C to +65°C)
- **Altitude**: 2000m or less
- **IP Rating**: IP 66 (with proper enclosure installation)
- **Case Materials**: Case = ABS Plastic, Lens = Polycarbonate
- **Ambient Humidity**: 35% to 85% RH (non-condensing)
- **Memory Backup upon Power Failure**: EEPROM writing up to 100,000 times; Memory duration: 10 years
- **Terminals**: Conforming Wiring 0.25-1.65mm² (24 to 16 AWG) Permitted Torque 0.5 N·m (0.369 ft·lb)

Agency Approvals

- UL508 listed (E311366), cULus, CE marked

Wiring

CTT-1C-D24

CTT-AN-D24

CTT-1C-A120

CTT-AN-A120
CTT Series - Digital Counter / Timer / Tachometer

Display, Indicators & Keys

CTT Series Dimensions

mm [inches]

Electronic parts list

For latest prices, please check AutomationDirect.com

Relays and Timers

1-800-633-0405