CTT Series - Digital Counter / Timer / Tachometer

Timer Mode

Timer Performance Specifications				
Timer Functions	Signal On Delay 1, Signal On Delay 2, Signal Off Delay, Signal On, Power On Delay, Power On Delay Hold, Repeat Cycle, Repeat Cycle Hold, Repeat Cycle 2, Signal Cumulate, Signal Twin On Start, Signal Twin Off Start (See time charts below).			
Number of Digits	6 digits on each line			
Display	Present values: red LED, character height 8mm; Set value: green LED, character height: 6mm			
Time Range	***Setting***	***Range***	***Units***	***Maximum***
	sec.	0.01 ~ 9,999.99	A unit = 10ms	9,999.99 secs.
	sec.	0.1 ~ 99,999.9	A unit = 0.1 sec.	99,999.9 secs.
	sec.	1 ~ 999,999	A unit = 1 sec.	999,999 secs.
	min., sec.	0.01 ~ 9,959.99	A unit = 0.01 sec.	5,999.99 secs.
	min., sec.	0.1 ~ 99,959.9	A unit = 0.1 sec.	59,999.9 secs.
	min.	0.1 ~ 99,999.9	A unit = 0.1 min.	99,999.9 mins.
	min.	1 ~ 999,999	A unit = 1 min.	999,999 mins.
	hr., min., sec.	1 ~ 995,959	A unit =1 sec.	359,999 secs. (100 hrs.)
	hr., min.	1 ~ 999,959	A unit =1 min.	35,999,999 secs. (10,000 hrs.)
	hr.	1 ~ 999,999	A unit = 1 hr.	699,999 hrs.
Display	Elapsed time / remaining time			
Timer	Power ON start max +0.01% w0.05 sec, Signal start max +0.01% w0.03 sec			
External Reset	Minimum reset input signal width 1ms or 20ms (selectable)			
Output Duration (flicker)	10-9990ms variable every 10ms			

Click on the above thumbnail or go to https://www.automationdirect.com/VID-RL-0008 for a short Timer demo video.

Click on the above thumbnail or go to https://www.automationdirect.com/VID-RL-0007 for a Timer Set-up video.

Timing Charts

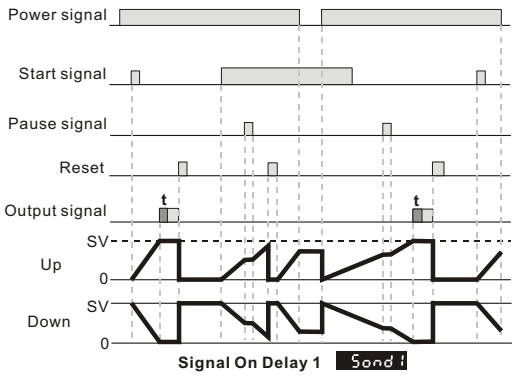
Signal On Delay 1 (Sond1)

With power applied to the CTT, the leading edge of the input signal at START will begin the timing period setting value SV (timing up or down based on parameter (t modE) or by DIP switch 2). At the end of the timing period both outputs will turn ON momentarily for the time set in the output pulse width parameter (tout1) or will be maintained ON if the output pulse width parameter (tout1) is set to 0.00. The trailing edge of the "start" signal has no effect on the outputs or timing period.

The leading edge of a "reset" input signal at RST1 will turn OFF the outputs and reset the timing period. The "reset" signal minimum pulse width is set by reset pulse width parameter (rtSr) or DIP Switch 8.

The leading edge of a "pause" input signal at GATE will pause the timing period after it has been started. The timing period will continue after the trailing edge of the external switch "pause" (Gate) signal.

When power is removed, both outputs will turn OFF and the timing period will be reset.



CTT Series - Digital Counter / Timer / Tachometer

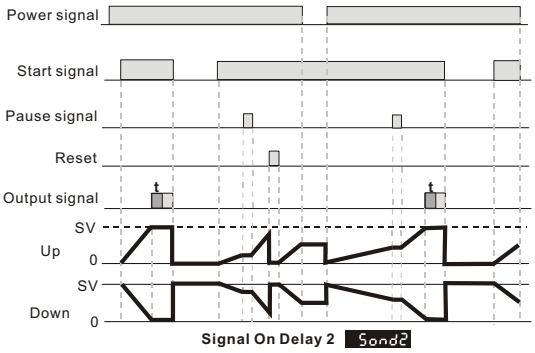
Signal On Delay 2 (Sond2)

With power applied to the CTT, the leading edge of the input signal at START will begin the timing period setting value SV (timing up or down based on parameter (t modE) or by DIP switch 2). At the end of the timing period both outputs will turn ON momentarily for the time set in the output pulse width parameter (tout1) or will be maintained ON if the output pulse width parameter (tout1) is set to 0.00. The trailing edge of the "start" signal will turn OFF the outputs and reset the timing period.

The leading edge of a "reset" input signal at RST1 will turn OFF the outputs and reset the timing period. The "reset" signal minimum pulse width is set by reset pulse width parameter (rtSr) or DIP Switch 8.

The leading edge of a "pause" input signal at GATE will pause the timing period after it has been started. The timing period will continue after the trailing edge of the external switch "pause" (Gate) signal.

When power is removed, both outputs will turn OFF and the timing period will be reset.



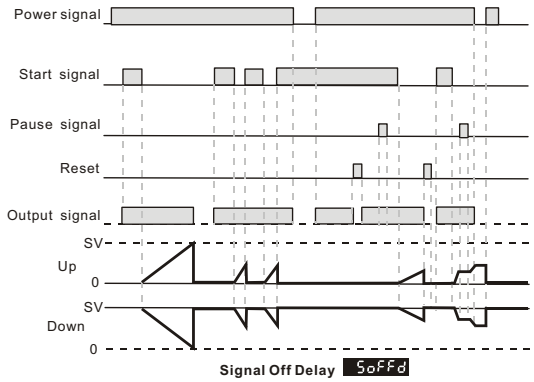
Signal Off Delay (Soffd)

With power applied to the CTT, the leading edge of the input signal at START will immediately turn ON the outputs. The trailing edge of the "start" signal will begin the timing period setting value SV (timing up or down based on parameter (t modE) or by DIP switch 2). At the end of the timing period both outputs will turn OFF. The leading edge of a "start" signal applied during a previously initiated timing period will reset the timing period.

The leading edge of a "reset" input signal at RST1 will turn OFF the outputs and reset the timing period. The "reset" signal minimum pulse width is set by reset pulse width parameter
(rtSr) or DIP Switch 8.

The leading edge of a "pause" input signal at GATE will pause the timing period after it has been started. The timing period will continue after the trailing edge of the external switch "pause" (Gate) signal.

When power is removed, both outputs will turn OFF and the timing period will be reset.



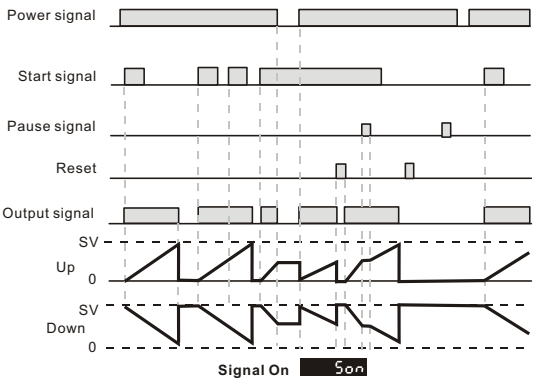
Signal On (Son)

With power applied to the CTT, the leading edge of the input signal at START will immediately turn ON the outputs and begin the timing period setting value SV (timing up or down based on parameter (t modE) or by DIP switch 2). The trailing edge of the "start" signal has no effect on the outputs or timing period. At the end of the timing period both outputs will turn OFF and the timing period will reset. The leading edge of a "start" signal applied during a previously initiated timing period will not reset the timing period.

The leading edge of a "reset" input signal at RST1 will turn OFF the outputs and reset the timing period. The "reset" signal minimum pulse width is set by reset pulse width parameter (rtSr) or DIP Switch 8.

The leading edge of a "pause" input signal at GATE will pause the timing period after it has been started. The timing period will continue after the trailing edge of the external switch "pause" (Gate) signal.

When power is removed, both outputs will turn OFF and the timing period will be reset.



CTT Series - Digital Counter / Timer / Tachometer

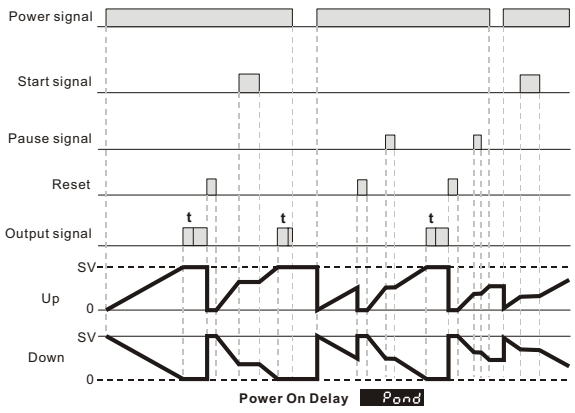
Power On Delay (Pond)

When power is applied to the CTT, the timing period setting value SV will begin (timing up or down based on parameter (t modE). At the end of the timing period both outputs will turn ON momentarily for the time set in the output pulse width parameter (tout1) or will be maintained ON if the output pulse width parameter (tout1) is set to 0.00.

The leading edge of a "reset" input signal at RST1 will turn OFF the outputs and reset the timing period. The "reset" signal minimum pulse width is set by reset pulse width parameter (rtSr).

The leading edge of a "pause" input signal at GATE or signal at START will pause the timing period after it has been started. The timing period will continue after the trailing edge of the external switch "pause" (Gate) or "start" signal.

When power is removed, both outputs will turn OFF and the timing period will be reset.



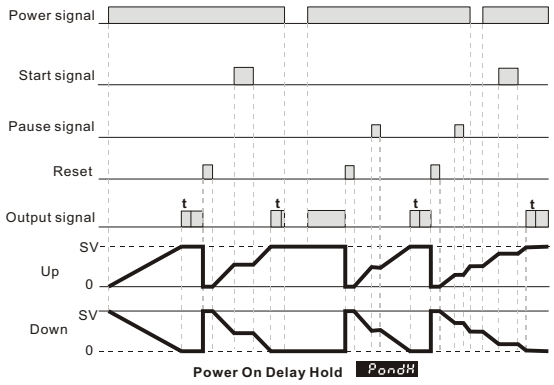
Power On Delay HOLD (PondH)

When power is applied to the CTT, the timing period setting value SV will begin (timing up or down based on parameter (t modE). At the end of the timing period both outputs will turn ON momentarily for the time set in the output pulse width parameter (tout1) or will be maintained ON if the output pulse width parameter (tout1) is set to 0.00.

The leading edge of a "reset" input signal at RST1 will turn OFF the outputs and reset the timing period. The "reset" signal minimum pulse width is set by reset pulse width parameter (rtSr).

The leading edge of a "pause" input signal at GATE or signal at START will pause the timing period after it has been started. The timing period will continue after the trailing edge of the "pause" (Gate) or "start" signal.

When power is removed, both outputs will turn OFF. The last state of the outputs and the last value of the current timing period will be "stored" in EEprom when power is removed. When power is reapplied the outputs will return to their last state and timing will resume from the last value of the timing period.



CTT Series - Digital Counter / Timer / Tachometer

Repeat Cycle (rCy)
With power applied to the CTT, the leading edge of the input signal at START will begin the timing period setting value SV (timing up or down based on parameter
(t modE). At the end of the timing period, the timing period will reset and repeat automatically.

If the output pulse width parameter (tout1) is set to 0.00 both outputs will turn ON at the end of the first timing period, turn OFF at the end of the next timing period, turn ON at the end of the next timing period, etc.

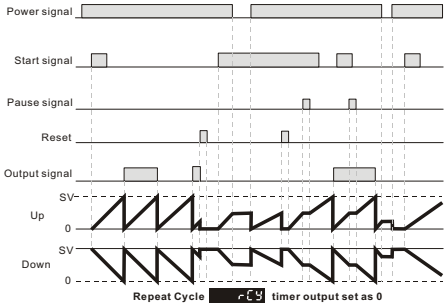
If the output pulse width parameter (tout1) is set to >0.00 both outputs will turn ON momentarily for the time set in the output pulse width parameter (tout1) at the beginning of the each timing period.

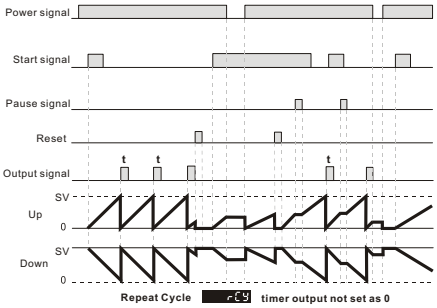
The trailing edge of the "start" signal has no effect on the outputs or timing period.

The leading edge of a "reset" input signal at RST1 will turn OFF the outputs and reset the timing period. The "reset" signal minimum pulse width is set by reset pulse width parameter (rtSr). The leading edge of a new "start" signal is necessary to restart the cycle.

The leading edge of a "pause" input signal at GATE will pause the timing period after it has been started. The timing period will continue after the trailing edge of the external switch "pause" (Gate) signal.

When power is removed, both outputs will turn OFF and the timing period will be reset.





Repeat Cycle HOLD (rCyH)
With power applied to the CTT, the leading edge of the input signal at START will begin the timing period setting value SV (timing up or down based on parameter (t modE). At the end of the timing period, the timing period will reset and repeat automatically.

If the output pulse width parameter (tout1) is set to 0, both outputs will turn ON at the end of the first timing period, turn OFF at the end of the next timing period, turn ON at the end of the next timing period, etc.

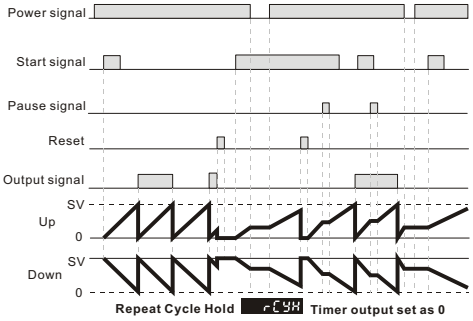
If the output pulse width parameter (tout1) is set to >0.00, both outputs will turn ON momentarily for the time set in the output pulse width parameter (tout1) at the beginning of the each timing period.

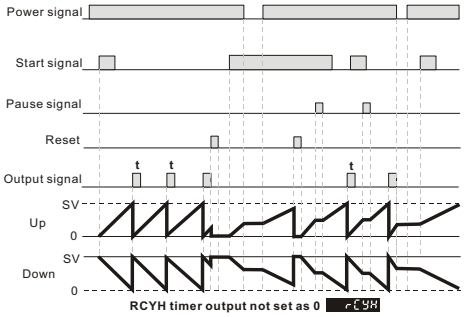
The trailing edge of the "start" signal has no effect on the outputs or timing period.

The leading edge of a "reset" input signal at RST1 will turn OFF the outputs and reset the timing period. The "reset" signal minimum pulse width is set by reset pulse width parameter (rtSr). The leading edge of a new "start" signal is necessary to restart the cycle.

The leading edge of a "pause" input signal at GATE will pause the timing period after it has been started. The timing period will continue after the trailing edge of the external switch "pause" (Gate) signal.

When power is removed, both outputs will turn OFF. The last state of the outputs and the last value of the current timing period will be "stored" in EEprom when power is removed. When power is reapplied the outputs will return to their last state and timing will resume from the last value of the timing period by the leading edge of a new "start" signal.





CTT Series - Digital Counter / Timer / Tachometer

Repeat Cycle 2 (rCy2)
With power applied to the CTT, the leading edge of the input signal at START will begin the timing period timing up or down based on parameter (t modE). At the end of the timing period, the timing period will reset and repeat automatically.

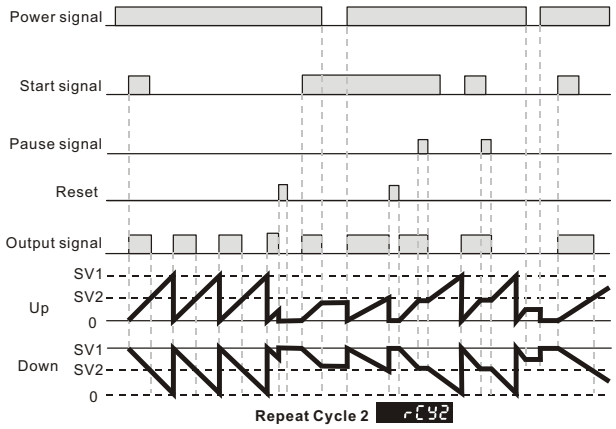
Both outputs will turn ON at the beginning of the first timing period and turn OFF when the timing period reaches time period setting SV2. The outputs will turn ON again when the time period reaches time period setting SV1.

The trailing edge of the "start" signal has no effect on the outputs or timing period.

The leading edge of a "reset" input signal at RST1 will turn OFF the outputs and reset the timing period. The "reset" signal minimum pulse width is set by reset pulse width parameter (rtSr). The leading edge of a new "start" signal is necessary to restart the cycle.

The leading edge of a "pause" input signal at GATE will pause the timing period after it has been started. The timing period will continue after the trailing edge of the external switch "pause" (Gate) signal.

When power is removed, both outputs will turn OFF and the timing period will be reset.

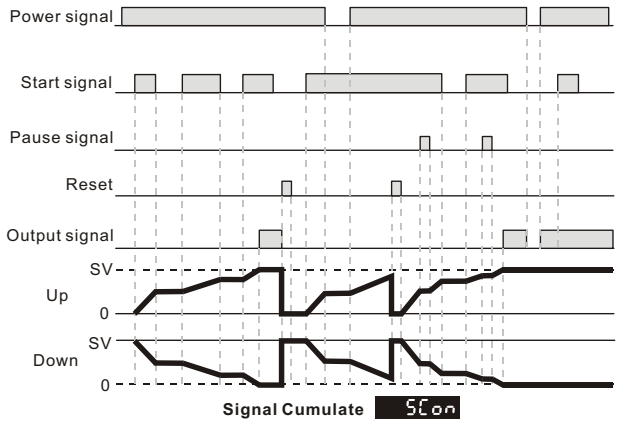


Signal Cumulate (SCon)
With power applied to the CTT, the leading edge of the input signal at START will begin the timing period setting value SV timing up or down based on parameter (t modE). The trailing edge of the "start" signal will pause the timing period. The leading edge of a subsequent "start" signal will resume timing from the last value of the timing period. At the end of the timing period both outputs will turn ON.

The leading edge of a "reset" input signal at RST1 will turn OFF the outputs and reset the timing period. The "reset" signal minimum pulse width is set by reset pulse width parameter (rtSr).

The leading edge of a "pause" input signal at GATE will pause the timing period after it has been started. The timing period will continue after the trailing edge of the external switch "pause" (Gate) signal.

When power is removed, both outputs will turn OFF. The last state of the outputs and the last value of the current timing period will be "stored" when power is removed. When power is reapplied the outputs will return to their last state and timing will resume from the last value of the timing period by the leading edge of a new "start" signal.



CTT Series - Digital Counter / Timer / Tachometer

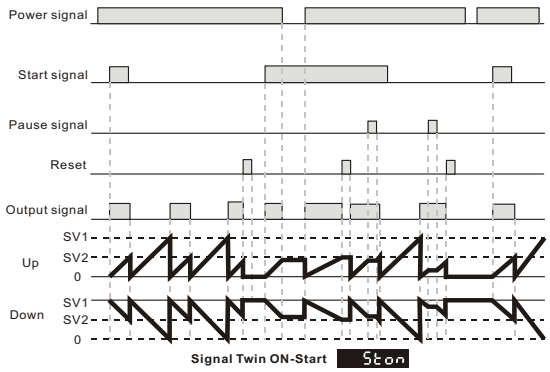
Signal Twin ON-Start (Ston)
With power applied to the CTT, the leading edge of the input signal at START will turn ON the outputs and begin the timing period timing up or down based on parameter (t modE). When the timing period reaches time setting SV2 the outputs will turn OFF and the time period will reset and restart automatically. When the time period now reaches time setting SV1 the outputs will turn ON again and the time period will reset and repeat automatically.

The trailing edge of the "start" signal has no effect on the outputs or timing period.

The leading edge of a "reset" input signal at RST1 will turn OFF the outputs and reset the timing period. The "reset" signal minimum pulse width is set by reset pulse width parameter (rtSr). The leading edge of a new "start" signal is necessary to restart the cycle.

The leading edge of a "pause" input signal at GATE will pause the timing period after it has been started. The timing period will continue after the trailing edge of the external switch "pause" (Gate) signal.

When power is removed, both outputs will turn OFF and the timing period will be reset.



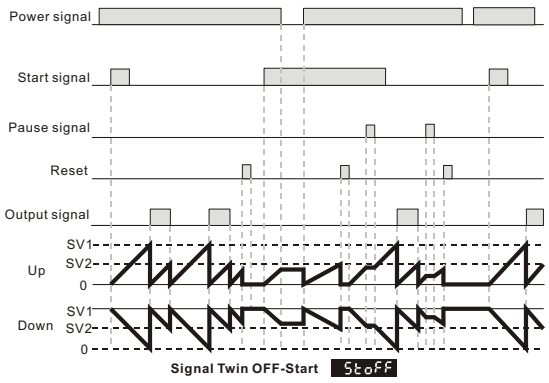
Signal Twin OFF-Start (StoFF)
With power applied to the CTT, the leading edge of an input signal at START will begin the timing period timing up or down based on parameter (t modE). When the timing period reaches time setting SV1 the outputs will turn ON and the time period will reset and restart automatically. When the time period now reaches time setting SV2 the outputs will turn OFF again and the time period will reset and repeat automatically.

The trailing edge of the "start" signal has no effect on the outputs or timing period.

The leading edge of a "reset" input signal at RST1 will turn OFF the outputs and reset the timing period. The "reset" signal minimum pulse width is set by reset pulse width parameter (rtSr). The leading edge of a new "start" signal is necessary to restart the cycle.

The leading edge of a "pause" input signal at GATE will pause the timing period after it has been started. The timing period will continue after the trailing edge of the external switch "pause" (Gate) signal.

When power is removed, both outputs will turn OFF and the timing period will be reset.



CTT Series - Digital Counter / Timer / Tachometer

Features

- Can operate as a digital counter, timer, combination timer + counter or tachometer
- Accepts voltage and non-voltage inputs from a wide variety of NPN, PNP, or dry contact sensors
- Selectable counting speeds from 1 to 10,000 cycles per second
- Multiple transistor and relay outputs can operate as momentary or maintained
- Double-line, 6-digit, 2-color LCD display
- Easy configuration with externally accessible DIP switches or the lockable keypad
- Display decimal point selection
- Available in 100-240VAC and 24VDC powered models
- UL508 listed (E311366), cULus, CE marked

E311366

A lot of functionality in one powerful little unit!

The CTT series is an extremely versatile multi-function device that is easily configured for operation as a digital counter, timer, combination timer + counter, or tachometer. Both voltage and non-voltage inputs are accepted from a wide variety of sensor types with NPN, PNP, or dry contact outputs. The first output on the CTT is a single-pole, single-throw relay and NPN transistor that operate concurrently. The second CTT output can be ordered as either a single-pole, double throw relay or NPN transistor. Parameters are easily set using the externally accessible DIP switches or the lockable keypad. The double-line, 6-digit, two-color LCD display shows the counter, timer, or tachometer present values, setting values and menu parameters during set-up. Additional individual indicators are provided for inputs, outputs and functions. The standard 1/16 DIN size, with included panel mounting clip and gasket, make panel mounting a snap. The CTT is available in 100-240VAC and 24VDC powered models.

Visit www.Automationdirect.com to download the free comprehensive CTT Series manual.

Counter/Timer/ Tachometer Functions

Counter Functions	Counter Input Modes	Counter Output Modes
1-Stage	Up	Select from eleven (11) different output modes (F, N, C, R, K, P, Q, A, S, T, D)
2-Stage	Down	
Batch	Up / Command Down	
Total	Up/ Down	
Dual	Quadrature	
	Addition	
	Subtraction	

Timer + Counter

Timer Functions (Up or Down)	Counter Input Modes	Counter Output Modes
Signal On Delay 1	Up	Select from eight (8) different output modes (F, N, C, R, K, P, Q, A)
Signal On Delay 2	Down	
Signal Off Delay		
Signal On		
Power On Delay		
Power On Delay Hold		
Repeat Cycle		
Repeat Cycle Hold		

Timer Functions (Up or Down)

Signal On Delay 1	Repeat Cycle
Signal On Delay 2	Repeat Cycle Hold
Signal Off Delay	Repeat Cycle 2
Signal On	Signal Cumulate
Power On Delay	Signal Twin On-Start
Power On Delay Hold	Signal Twin Off-Start

Tachometer Output Modes

Select from four (4) different output modes
2Lo/1Lo
2Lo/1Hi
2Hi/1Lo
2Hi/1Hi

Click on the above thumbnail or go to https://www.automationdirect.com/VID-RL-0001 for a short introductory video for the CTT units.

For a full set of Demo and Set Up videos for the CTT units please scan the QR code or follow the link below.
https://www.automationdirect.com/videos/home?t=link&-cat1=60

CTT Series - Digital Counter / Timer / Tachometer

Digital Counter / Timer / Tachometer			
Part Number	***Description***	***Wt (lb)***	***Price***
CTT-AN-D24	Counter / Timer / Tachometer, Output 1 NPN & SPST relay, Output 2 NPN, 24 VDC powered, panel mounting clip is included*	0.4	$;-00d!l:
CTT-AN-A120	Counter / Timer / Tachometer, Output 1 NPN & SPST relay, Output 2 NPN, 100-264 VAC powered, panel mounting clip is included*	0.4	$;00d!k:
CTT-1C-D24	Counter / Timer / Tachometer, Output 1 NPN & SPST relay, Output 2 SPDT relay, 24 VDC powered, panel mounting clip is included*	0.4	$;-00d!j:
CTT-1C-A120	Counter / Timer / Tachometer, Output 1 NPN & SPST relay, Output 2 SPDT relay, 100-264 VAC powered, panel mounting clip is included*	0.4	$;-00d!i:

*** Spare panel clips part number PANEL-16**

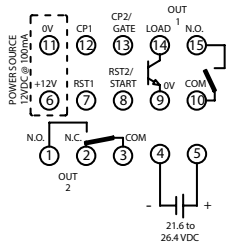
Digital Counter / Timer / Tachometer General Specifications			
Input Power Requirements		100 to 240 VAC 50/60 Hz	24 VDC
Operation Voltage Range		85 to 264 VAC	21.6 to 26.4 VDC
Power Consumption		Less than 10VA	
Power Source		12VDC +10%, 100mA	
Display		Double-line, 6-digit LCD display (SV = 8mm, PV = 6mm)	
Input Signal		NPN ON impedance 1K ohm max. ON residual voltage: 2V max. PNP 4.5 to 30VDC, low level: 0 to 2VDC	
		Counting Speed Setting (Count per second)	Minimum Input Signal Width (Milliseconds)
		1cps	20ms
		30cps	16.7 ms
		1K cps	0.5 ms
		5K cps	0.1 ms
		10K cps	0.05 ms
Output 1		Relay: SPST max. 250VAC, 5A (resistive load), 4A (inductive load); Transistor: NPN open collector. When 100mA @ 30VDC, residual voltage = 1.5VDC max	
Output 2	***CTT-1C-xxx***	Relay: SPDT max. 250VAC/30VDC, 5A (resistive load), 4A (inductive load)	
	CTT-AN-xxx	Transistor: NPN open collector. When 100mA @ 30VDC residual voltage = 1.5VDC max	
Life Expectancy	***Mechanical***	10,000,000 operations (frequency 18,000 operations/hr)	
	Electrical	100,000 operations (frequency 900 operations/hr)	
Output Duration (where used)		0.00 (latching) / 0.01 to 99.99 seconds	
Output Switching Time		2 milliseconds max	
Dielectric Strength		2000VAC 50/60 Hz for 1 minute	
Vibration Resistance		Without damage: 10 ~ 55 Hz, amplitude = 0.75 mm, 3 axes for 2 hours	
Shock Resistance		Without damage: drop 4 times, 300m/s^2 3 edges, 6 surfaces and 1 corner	
Ambient Temperature		+32 to +122°F (0 to +50°C)	
Storage Temperature		-4 to +149°F (-20 to +65°C)	
Altitude		2000m or less	
IP Rating		IP 66 (with proper enclosure installation)	
Case Materials		Case = ABS Plastic, Lens = Polycarbonate	
Ambient Humidity		35% to 85% RH (non-condensing)	
Memory Backup upon Power Failure		EEPROM writing up to 100,000 times; Memory duration: 10 years	
Terminals	***Conforming Wiring***	0.25-1.65mm² (24 to 16 AWG)	
	Permitted Torque	0.5 N·m (0.369 ft·lb)	
Agency Approvals *		UL508 listed (E311366), cULus, CE marked	

*** To obtain the most current agency approval information, see the Agency Compliance & Certifications Checklist section on the specific part number's web page.**

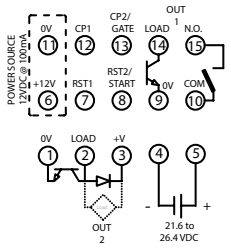
CTT Series - Digital Counter / Timer / Tachometer

Wiring Diagrams

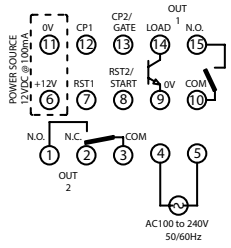
CTT-1C-D24



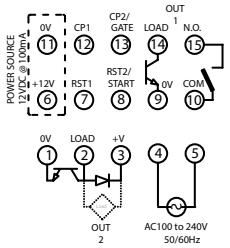
CTT-AN-D24



CTT-1C-A120

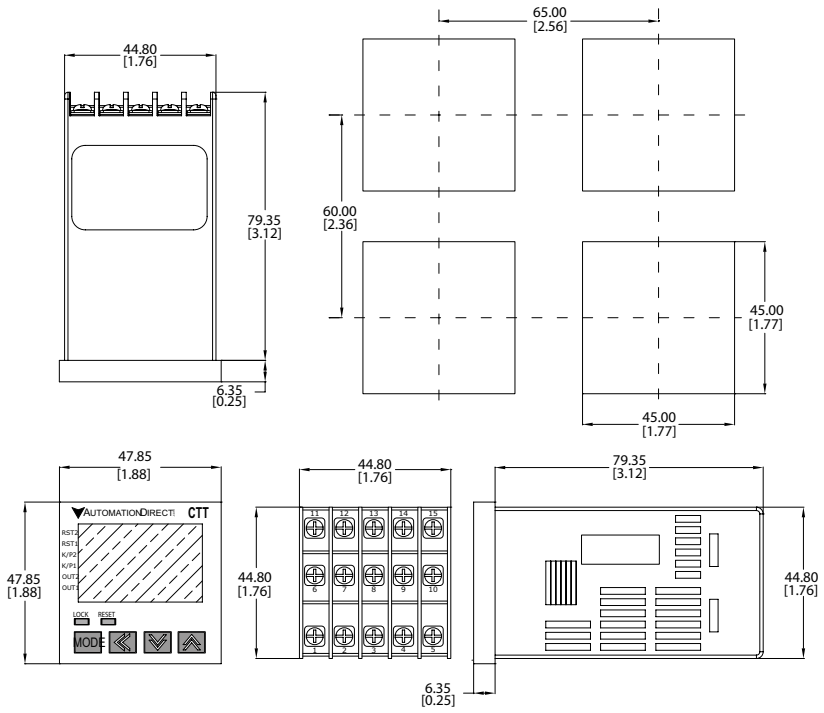


CTT-AN-A120



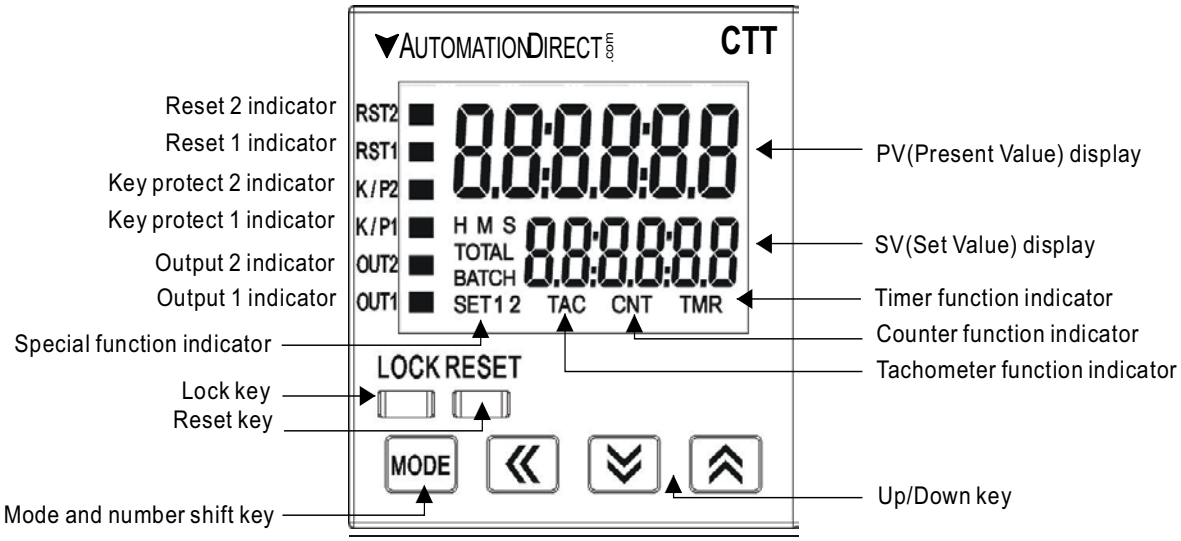
Dimensions

mm [inches]



CTT Series - Digital Counter / Timer / Tachometer

Display, Indicators & Keys



LCD Display and Indicators			
RST 1/2	Light on when reset signal is detected	***BATCH***	"Batch Counting Mode" in Counter
K/P 1/2	Light on when key-protected mode is enabled	***SET 1 2***	SV1, SV2 display
OUT 1/2	Light on when output is executing	***TAC***	Light on in Tachometer function
H M S	Hour, minute, second, unit of timer, displayed in Timer function	***CNT***	Light on in Counter function
TOTAL	"Total Counting Mode" in Counter function	***TMR***	Light on in Timer function