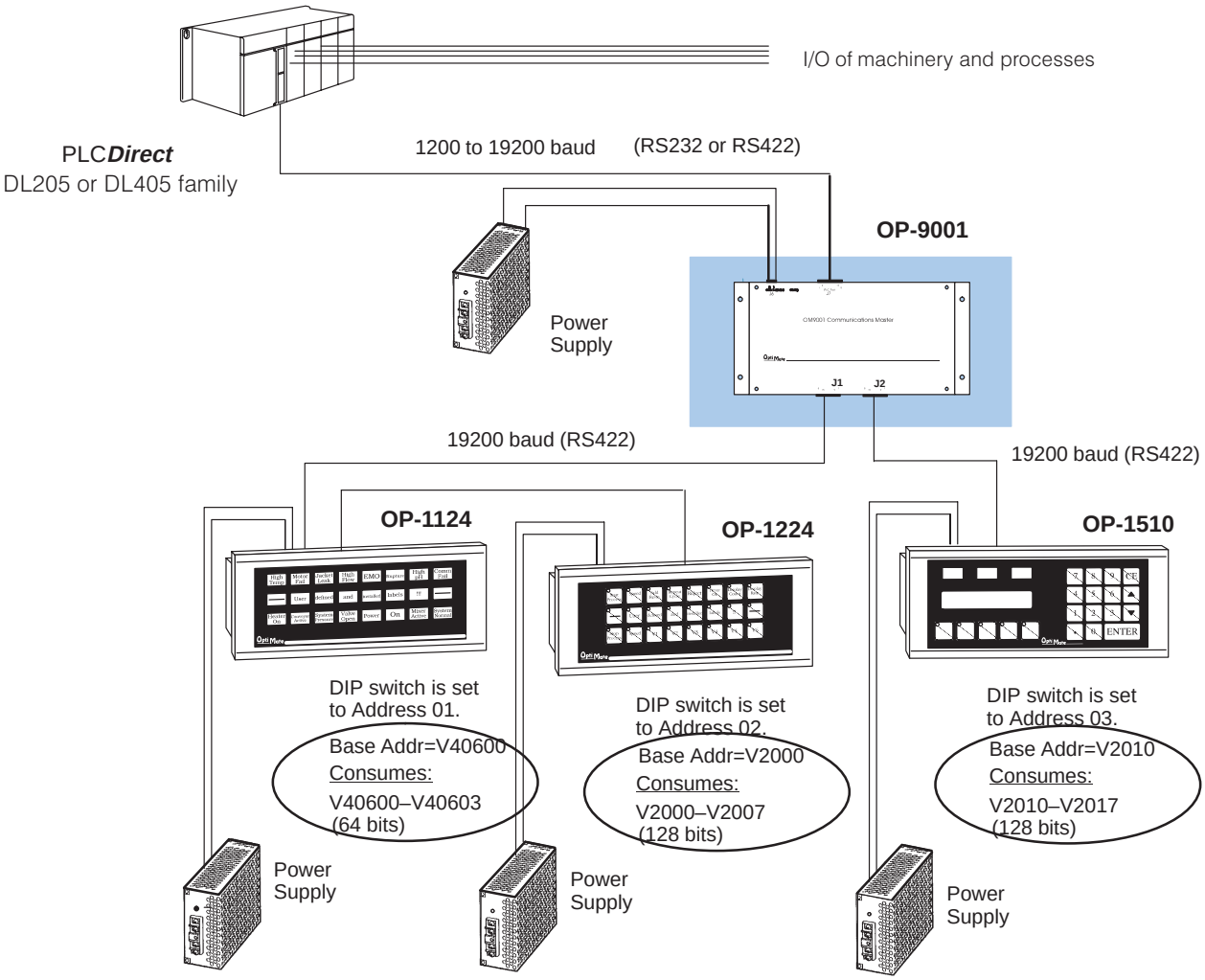
Planning Your Memory Mapping

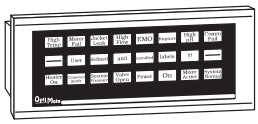
When using more than one OP-panel in a system, it is important that you plan ahead to make sure the memory mapping for one panel does not overwrite the memory mapping for another panel. Let's take a look again at a typical system. Notice that each panel shown consumes a fixed amount of memory for its mapping. For example, The OP-1124 needs 64 consecutive bits; the OP-1224 needs 128 consecutive bits; and the OP-1510 needs 128 consecutive bits. When you are planning your system, you have to make sure that your panels don't compete for the same memory space. To help you with this process, we have given you a memory assignment template on Page 7. We have also included a chart on Page 6 that shows you the memory requirements for each of the currently available OP-panels.



Memory Consumption for Mapping Process

NOTE: For PLC*Direct* and compatibles, remember that the V-Memory and R-Memory addresses are numbered in octal–not decimal. For example, V2007 and V2010 are consecutive registers–V2008 and V2009 do not exist.

OP-1124

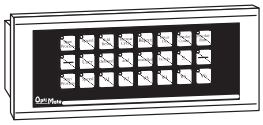


Consumes 64 consecutive bits:
4 sixteen bit registers (DL205/DL405 and A-B)
8 eight bit registers (DL305 only)

Data Registers

	DL205/DL405	DL305	A-B	Function
m	1	2	1	Lamps 1-16 ON/OFF
m+1	1	2	1	Lamps 17-24 ON/OFF
m+2	1	2	1	Lamps 1-16 flash
m+3	1	2	1	Lamps 17-24 flash

OP-1224

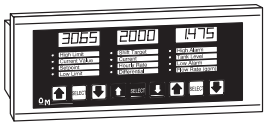


Consumes 128 consecutive bits:
8 sixteen bit registers (DL205/DL405 and A-B)
16 eight bit registers (DL305 only)

Data Registers

	DL205/DL405	DL305	A-B	Function
n	1	2	1	Pushbuttons 1-16 ON/OFF
n+1	1	2	1	Pushbuttons 17-24 ON/OFF
n+2	1	2	1	LEDs 1-16 flash
n+3	1	2	1	LEDs 17-24 flash
n+4	1	2	1	LEDs 1-16 ON/OFF
n+5	1	2	1	LEDs 17-24 ON/OFF
n+6	1	2	1	Force Function Data (1-16)
n+7	1	2	1	Force Function Mode/Data (17-24)

OP-1312

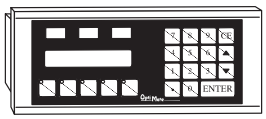


Consumes 224 consecutive bits:
14 sixteen bit registers (DL205/DL405 and A-B)
28 eight bit registers (DL305 only)

Data Registers

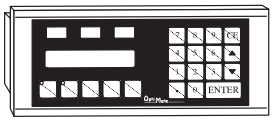
	DL205/DL405	DL305	A-B	Function
p	1	2	1	Location 1 data
p+1	1	2	1	Location 2 data
p+2	1	2	1	Location 3 data
p+3	1	2	1	Location 4 data
p+4	1	2	1	Location 5 data
p+5	1	2	1	Location 6 data
p+6	1	2	1	Location 7 data
p+7	1	2	1	Location 8 data
p+8	1	2	1	Location 9 data
p+9	1	2	1	Location 10 data
p+10	1	2	1	Location 11 data
p+11	1	2	1	Location 12 data
p+12	1	2	1	Force data flags
p+13	1	2	1	Data to be forced

OP-1500



Consumes 128 consecutive bits:
8 sixteen bit registers (DL205/DL405 and A-B)
16 eight bit registers (DL305 only)

OP-1510



Data Registers

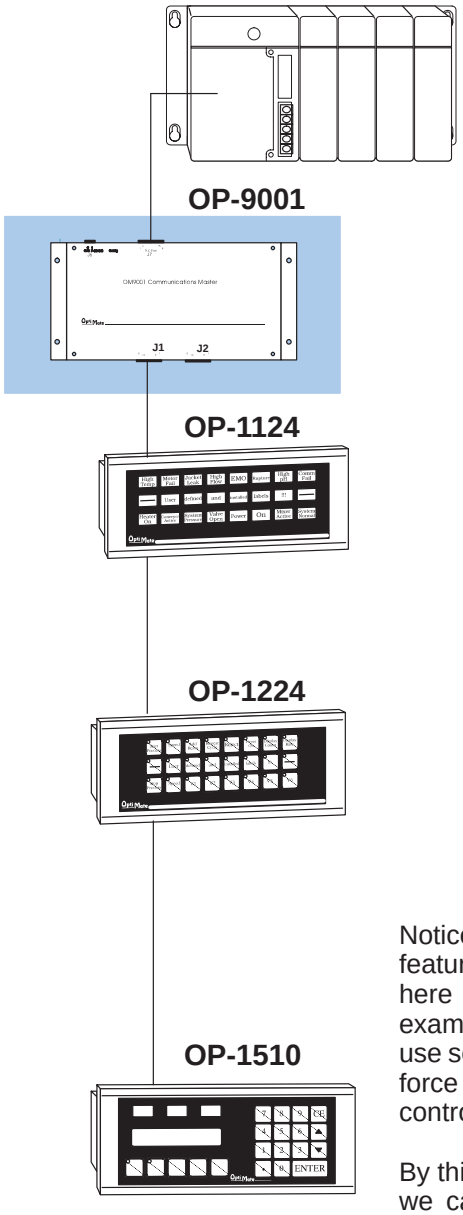
	DL205/DL405	DL305	A-B	Function
q	1	2	1	Top line message selection
q+1	1	2	1	Bottom line message selection
q+2	1	2	1	Top line data/menu function*
n+3	1	2	1	Decimal point, top line
q+4	1	2	1	Bottom line data
q+5	1	2	1	Decimal point, bottom line
q+6	1	2	1	Status register
q+7	1	2	1	Control register

*q+2 holds Function Number for the OP-1510 only. See OP-1510–M manual.

Using a Memory Planner

On Page 7, we have included a template for planning your memory mapping in a multi-panel configuration. The following example shows the memory requirements and assignments for three OP-panels connected to a DL405 programmable controller. Refer to the chart on Page 5 to find out how many registers of consecutive memory are required for each panel. Memory does not have to be consecutive between the various panels.

DL405



OP-Panel Memory Planner

PLC Address for OP-9001 1

Panel Number (0--30)	Panel Name	Words Needed	Original Mapping		Remapping	
			Base Address	Final Word Address	Relationship	Function
1	OP-1124	4	V40600	V40603		
2	OP-1224	8	V2000	V2007		
					V2000:V40600	Pushbuttons 1-16
					V2001:V40601	Pushbuttons 17-24
3	OP-1510	8	V2010	V2017		
					V2016:V40602	Status Register
					V2017:V40603	Control Register

Notice that we have remapped some addresses to take advantage of select features that require individual bit manipulation.We have kept things simple here to make the example easy to understand. For the OP-1224, for example, we have only remapped the pushbuttons, and have elected not to use some other features that would require remapping, i.e. LED separation, force function, etc. On the other hand, we have remapped the status and control registers of the OP-1510.

By thinking out memory allocation for the original mapping and remapping, we can prevent possible memory overlap in either area. Refer to your respective OP-panel User Manuals to determine what features need to make use of remapping. Remapping is never an issue with the DL450 or Allen-Bradley PLCs because of bit-of-word capability. For these PLCs ignore this part of the template.

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OP-Panel Memory Planner

PLC Address for OP-9001_____

Panel Number (0 – 30)	Panel Name	Registers Needed	**Original Mapping**		**Remapping**	
			Base Address	Final Word Address	Relationship	Function