CPU Specifications and Operations

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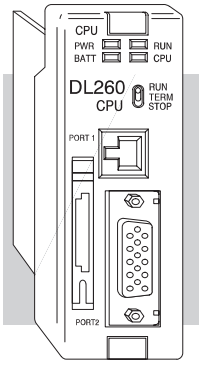
CPU Overview



The Central Processing Unit is the heart of the PLC. Almost all system operations are controlled by the CPU, so it is important that it is set up and installed correctly. This chapter provides the information needed to understand:

- The differences between the various models of CPUs, and
- The steps required to set up and install the CPU.

General CPU Features

The DL230, DL240, DL250–1 and D2–260 are modular CPUs which can be installed in 3, 4, 6, or 9 slot bases. All I/O modules in the DL205 family will work with any of the CPUs. The DL205 CPUs offer a wide range of processing power and program instructions. All offer RLL and Stage program instructions (See Chapter 5). They also provide extensive internal diagnostics that can be monitored from the application program or from an operator interface.

DL230 CPU Features

The DL230 has 2.4K words of memory comprised of 2.0K of ladder memory and approximately 400 words of V-memory (data registers). It has 92 different instructions available for programming, and supports a maximum of 256 I/O points.

Program storage is in the factory-installed EEPROM. In addition to the EEPROM there is also RAM on the CPU which will store system parameters, V-memory, and other data which is not in the application program.

The DL230 provides one built-in RS-232 communication port, so you can easily connect a handheld programmer or a personal computer without needing any additional hardware.

DL240 CPU Features

The DL240 has a maximum of 3.8K of memory comprised of 2.5K of ladder memory and approximately 1.3K of V-memory (data registers). There are 129 instructions available for program development and a maximum of 256 points local I/O, and 896 points with remote I/O are supported.

Program storage is in the factory-installed EEPROM. In addition to the EEPROM, there is also RAM on the CPU that will store system parameters, V-memory and other data which is not in the application program.

The DL240 has two communication ports. The top port is the same port configuration as the DL230. The bottom port also supports the ***Direct***NET protocol, so you can use the DL240 in a ***Direct***NET network. Since the port is RS-232, you must use an RS-232/RS-422 converter for multi-drop connections.

DL250–1 CPU Features

The DL250–1 replaces the DL250 CPU. It offers all the DL240 features, plus more program instructions and a built–in Remote I/O Master port. It offers all the features of the DL250 CPU with the addition of supporting Local expansion I/O. It has a maximum of 14.8K of program memory comprised of 7.6K of ladder memory and 7.2K of V-memory (data registers). It supports a maximum of 256 points of local I/O and a maximum of 768 I/O points (maximum of two local expansion bases). In addition, port 2 supports up to 2048 points if you use the DL250–1 as a Remote master. It includes an internal RISC–based microprocessor for greater processing power. The DL250–1 has 240 instructions. The instructions are in addition to the DL240 instruction set which includes drum timers, a print function, floating point math, PID loop control for 4 loops and the Intelligent Box (IBox) instructions.

The DL250–1 has a total of two built–in communications ports. The top port is identical to the top port of the DL240, with the exception of the ***Direct***Net slave feature. The bottom port is a 15–pin RS-232/RS-422 port. It will interface with ***Direct***SOFT and operator interfaces, and provides ***Direct***Net and Modbus RTU Master/Slave connections.

DL260 CPU Features

The DL260 offers all the DL250–1 features, plus ASCII IN/OUT and expanded Modbus instructions. It also supports up to 1280 local I/O points by using up to four local expansion bases. It has a maximum of 30.4K of program memory comprised of 15.8K of ladder memory (saved on flash memory) and 14.6K of V-memory (data registers). It also includes an internal RISC–based microprocessor for greater processing power. The DL260 has 297 instructions. In addition to those in the DL250–1 instruction set, the DL260 instruction set includes table instructions, trigonometric instructions and support for 16 PID loops.

The DL260 has a total of two built–in communications ports. The top port is identical to the top port of the DL250–1. The bottom port is a 15–pin RS-232/RS-422/RS-485 port. It will interface with ***Direct***SOFT (version 4.0 or later), operator interfaces, and provides ***Direct***Net, Modbus RTU Master/Slave connections. Port 2 also supports ASCII IN/OUT instructions.

CPU General Specifications

Feature	DL230	DL240	DL250–1	DL260
Total Program memory (words)	2.4K	3.8K	14.8K	30.4K
Ladder memory (words)	2048	2560	7680 (Flash)	15872 (Flash)
V-memory (words)	256	1024	7168	14592
Non-volatile V Memory (words)	128	256	No	No
Boolean execution /K	4–6 ms	10–12 ms	1.9 ms	1.9 ms
RLL and RLL^{PLUS} Programming	Yes	Yes	Yes	Yes
Handheld programmer	Yes	Yes	Yes	Yes
*Direct*SOFT programming for Windows.	Yes	Yes	Yes	Yes (requires version 4.0 or higher)
Built-in communication ports	One RS–232	Two RS–232	One RS–232 One RS–232 or RS–422	One RS–232 One RS–232, RS–422 or RS–485
EEPROM	Standard on CPU	Standard on CPU	Flash	Flash
Total CPU memory I/O points available	256 (X,Y,CR)	896 (X, Y, CR)	2048 (X, Y, CR)	8192 (X, Y, CR, GX, GY)
Local I/O points available	256	256	256	256
Local Expansion I/O points (including local I/O and expansion I/O points)	N/A	N/A	768 (2 exp. bases max.)	1280 (4 exp. bases max.)
Serial Remote I/O points (including local I/O and expansion I/O points)	N/A	896	2048	8192
Serial Remote I/O Channels	N/A	2	8	8
Max Number of Serial Remote Slaves	N/A	7 Remote / 31 Slice	7 Remote / 31 Slice	7 Remote / 31 Slice
Ethernet Remote I/O Discrete points	N/A	896	2048	8192
Ethernet Remote I/O Analog I/O channels	N/A	Map into V–memory	Map into V–memory	Map into V–memory
Ethernet Remote I/O channels	N/A	Limited by power budget	Limited by power budget	Limited by power budget
Max Number of Ethernet slaves per channel	N/A	16	16	16
I/O points per Remote channel	N/A	16,384 (limited to 896 by CPU)	16,384 (16 fully expanded H4–EBC slaves using V–memory and bit–of–word instructions)	16,384 (16 fully expanded H4–EBC slaves using V–memory and bit–of–word instructions
I/O Module Point Density	4/8/12/16/32	4/8/12/16/32	4/8/12/16/32	4/8/12/16/32
Slots per Base	3/4/6/9	3/4/6/9	3/4/6/9	3/4/6/9

Feature	DL230	DL240	DL250–1	DL260
Number of instructions available (see Chapter 5 for details)	92	129	240	297
Control relays	256	256	1024	2048
Special relays (system defined)	112	144	144	144
Stages in RLL^{PLUS}	256	512	1024	1024
Timers	64	128	256	256
Counters	64	128	128	256
Immediate I/O	Yes	Yes	Yes	Yes
Interrupt input (hardware / timed)	Yes / No	Yes / Yes	Yes / Yes	Yes / Yes
Subroutines	No	Yes	Yes	Yes
Drum Timers	No	No	Yes	Yes
Table Instructions	No	No	No	Yes
For/Next Loops	No	Yes	Yes	Yes
Math	Integer	Integer	Integer, Floating Point	Integer, Floating Point, Trigonometric
ASCII	No	No	Yes, OUT	Yes, IN/OUT
PID Loop Control, Built In	No	No	Yes, 4 Loops	Yes, 16 Loops
Time of Day Clock/Calendar	No	Yes	Yes	Yes
Run Time Edits	Yes	Yes	Yes	Yes
Supports Overrides	No	Yes	Yes	Yes
Internal diagnostics	Yes	Yes	Yes	Yes
Password security	Yes	Yes	Yes	Yes
System error log	No	Yes	Yes	Yes
User error log	No	Yes	Yes	Yes
Battery backup	Yes (optional)	Yes (optional)	Yes (optional)	Yes (optional)

CPU Base Electrical Specifications

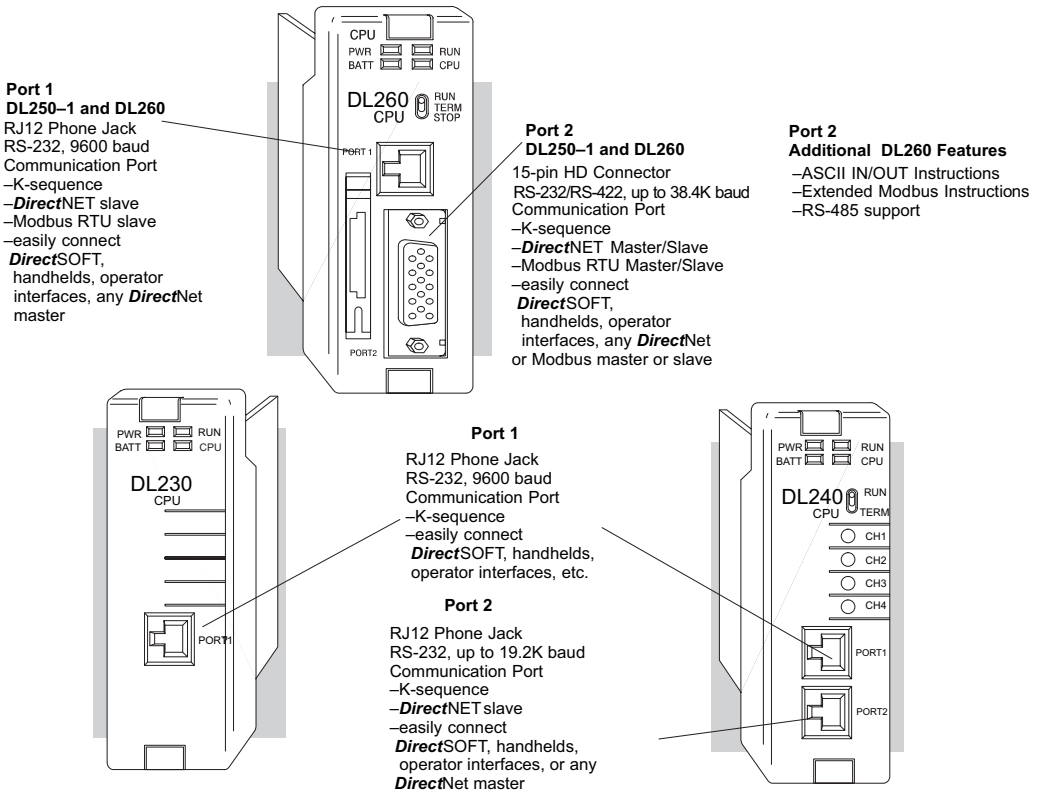
Specification	AC Powered Bases	24 VDC Powered Bases	125 VDC Powered Bases
Part Numbers	D2–03B–1 D2–04B–1 D2–06B–1 D2–09B–1	D2–03BDC1–1 D2–04BDC1–1 D2–06BDC1–1 D2–09BDC1–1	D2–06BDC2–1 D2–09BDC2–1
Input Voltage Range	100–240 VAC +10% –15%	10.2–28.8 VDC (24VDC) with less than 10% ripple	104–240 VDC +10% –15%
Maximum Inrush Current	30A	10A	20A
Maximum Power	80VA	25W	30W
Voltage Withstand (dielectric)	1 minute @ 1500VAC between primary, secondary, field ground, and run relay		
Insulation Resistance	> 10MΩ at 500VDC		
Auxiliary 24 VDC Output	20–28 VDC, less than 1V p-p 300mA max.	None	20–28 VDC, less than 1V p-p 300mA max.
Fusing (internal to base power supply)	Non–replaceable 2A @ 250V slow blow fuse	Non–replaceable 3.15 A @ 250V slow blow fuse	Non–replaceable 2A @ 250V slow blow fuse

CPU Hardware Setup

Communication Port Pinout Diagrams

Cables are available that allow you to quickly and easily connect a Handheld Programmer or a personal computer to the DL205 CPUs. However, if you need to build a cable(s), use the pinout descriptions shown on the following pages. You can also use the Tech Support/Cable Wiring diagrams located on our website.

The DL240, DL250–1 and DL260 CPUs have two ports while the DL230 has only one. All of the CPUs require at least one RJ-12 connector. The DL250-1 and DL260 require one 15 pin D-shell connector.

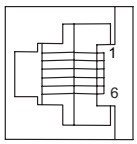


Port 1 Specifications

☑ 230
☑ 240
☒ 250-1
☒ 260

The operating parameters for Port 1 on the DL230 and DL240 CPUs are fixed.

- 6-pin female modular (RJ12 phone jack) type connector
- K–sequence protocol (slave only)
- RS-232, 9600 baud
- Connect to *Direct*SOFT, D2–HPP, DV–1000, HMI panels
- Fixed station address of 1
- 8 data bits, one stop
- Asynchronous, Half–duplex, DTE
- Odd parity



6-pin Female
Modular Connector

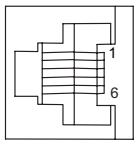
Port 1 Pin Descriptions (DL230 and DL240)		
1	0V	Power (–) connection (GND)
2	5V	Power (+) connection
3	RXD	Receive Data (RS-232)
4	TXD	Transmit Data (RS-232)
5	5V	Power (+) connection
6	0V	Power (–) connection (GND)

Port 1 Specifications

☒ 230
☒ 240
☑ 250-1
☑ 260

The operating parameters for Port 1 on the DL250–1 and DL260 CPU are fixed. This applies to the DL250 as well.

- 6-pin female modular (RJ12 phone jack) type connector
- K–sequence protocol (slave only)
- *Direct*NET (slave only)
- Modbus RTU (slave only) - supported only on D2-250-1 and D2-260
- RS-232, 9600 baud
- Connect to *Direct*SOFT, D2–HPP, DV1000 or *Direct*NET master
- 8 data bits, one start, one stop
- Asynchronous, Half–duplex, DTE
- Odd parity



6-pin Female
Modular Connector

Port 1 Pin Descriptions (DL250-1 and DL260)		
1	0V	Power (–) connection (GND)
2	5V	Power (+) connection
3	RXD	Receive Data (RS-232C)
4	TXD	Transmit Data (RS-232C
5	5V	Power (+) connection
6	0V	Power (–) connection (GND)

NOTE: *The 5V pins are rated at 200mA maximum, primarily for use with some operator interface units.*

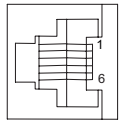
Port 2 Specifications

☒ 230
☑ 240
☒ 250-1
☒ 260

3

The operating parameters for Port 2 on the DL240 CPU are configurable using Aux functions on a programming device.

- 6-Pin female modular (RJ12 phone jack) type connector
- K–sequence protocol, *Direct*NET (slave),
- RS-232, Up to 19.2K baud
- Address selectable (1–90)
- Connect to *Direct*SOFT, D2–HPP, DV-1000, HMI, or *Direct*NET master
- 8 data bits, one start, one stop
- Asynchronous, Half–duplex, DTE
- Odd or no parity



6-pin Female
Modular Connector

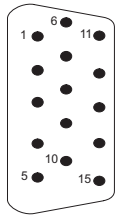
Port 2 Pin Descriptions (DL240 only)		
1	0V	Power (–) connection (GND)
2	5V	Power (+) connection
3	RXD	Receive Data (RS-232)
4	TXD	Transmit Data (RS-232)
5	RTS	Request to Send
6	0V	Power (–) connection (GND)

Port 2 Specifications

☒ 230
☒ 240
☑ 250-1
☑ 260

Port 2 on the DL250-1 and DL260 CPUs is located on the 15-pin D-shell connector. It is configurable using AUX functions on a programming device. This applies to the DL250 as well.

- 15-Pin female D type connector
- Protocol: K-sequence, *Direct*NET Master/ Slave, Modbus RTU Master/Slave, Remote I/O, (ASCII IN/OUT DL260 only)
- RS-232, non-isolated, distance within 15m (approximately 50ft)
- RS-422, non-isolated, distance within 1000 m (approximately 3280ft)
- RS-485, non–isolated, distance within 1000m (DL260 only
- Up to 38.4 K baud
- Address selectable (1–90)
- Connects to *Direct*SOFT, D2–HPP, operator interfaces, any *Direct*NET or Modbus master/slave, (ASCII devices-DL260 only)
- 8 data bits, one start, one stop
- Asynchronous, Half–duplex, DTE Remote I/O
- Odd/even/none parity



15-pin Female
D Connector

Port 2 Pin Descriptions (DL250–1 / DL260)		
1	5V	5VDC
2	TXD2	Transmit Data (RS-232)
3	RXD2	Receive Data (RS-232)
4	RTS2	Ready to Send (RS–232)
5	CTS2	Clear to Send (RS–232)
6	RXD2 –	Receive Data – (RS–422) (RS–485 DL260)
7	0V	Logic Ground
8	0V	Logic Ground
9	TXD2 +	Transmit Data + (RS–422) (RS–485 DL260)
10	TXD2 –	Transmit Data – (RS–422) (RS–485 DL260)
11	RTS2 +	Request to Send + (RS–422) (RS–485 DL260)
12	RTS2 –	Request to Send – (RS–422)(RS–485 DL260)
13	RXD2 +	Receive Data + (RS–422) (RS–485 DL260)
14	CTS2 +	Clear to Send + (RS422) (RS–485 DL260)
15	CTS2 –	Clear to Send – (RS–422) (RS–485 DL260)

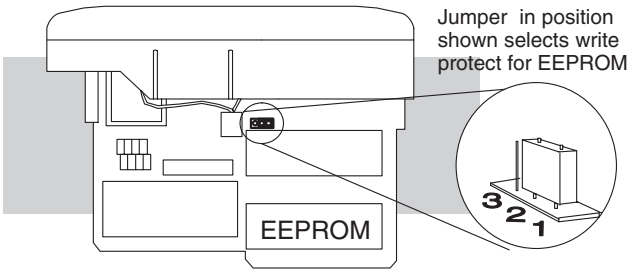
Selecting the Program Storage Media

Built-in EEPROM

☑ 230
☑ 240
☒ 250-1
☒ 260

The DL230 and DL240 CPUs provide built-in EEPROM storage. This type of memory is non-volatile and is not dependent on battery backup to retain the program. The EEPROM can be electrically reprogrammed without being removed from the CPU. You can also set Jumper 3, which will write protect the EEPROM. The jumper is set at the factory to allow changes to EEPROM. If you select write protection by changing the jumper position, you cannot make changes to the program.

WARNING: Do NOT change Jumper 2. This is for factory test operations. If you change Jumper 2, the CPU will not operate properly.



EEPROM Sizes

The DL230 and DL240 CPUs use different sizes of EEPROMs. The CPUs come from the factory with EEPROMs already installed. However, if you need extra EEPROMs, select one that is compatible with the following part numbers.

CPU Type	EEPROM Part Number	Capacity
DL230	Hitachi HN58C65P–25	8K byte (2Kw)
DL240	Hitachi HN58C256P–20	32K byte (3Kw)

EEPROM Operations

Many AUX functions are specifically for use with an EEPROM in the Handheld Programmer. This enables you to quickly and easily copy programs between a program developed offline in the Handheld Programmer and the CPU. Also, you can erase EEPROMs, compare them, etc. See the DL205 Handheld Programmer Manual for details on using these AUX functions with the Handheld Programmer.

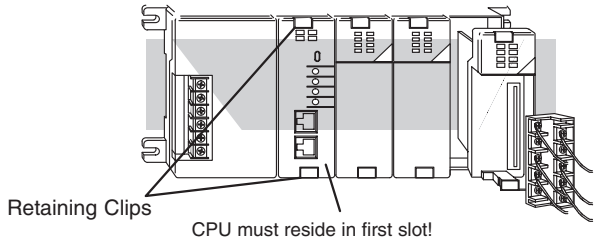
NOTE: *If the instructions are supported in both CPUs and the program size is within the limits of the DL230, you can move a program between the two CPUs. However, the EEPROM installed in the Handheld Programmer must be the same size as (or larger than) the CPU being used. For example, you could not install a DL240 EEPROM in the Handheld Programmer and download the program to a DL230. Instead, if the program is within the size limits of the DL230, use a DL230 chip in the Handheld when you obtain the program from the DL240.*

Installing the CPU

☑ 230
☑ 240
☑ 250-1
☑ 260

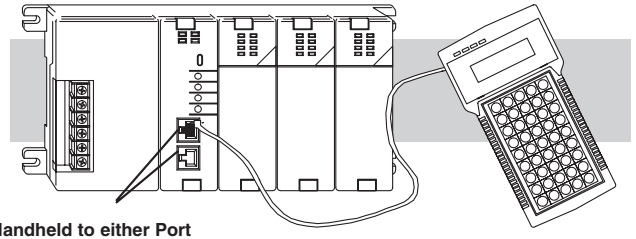
The CPU must be installed in the first slot in the base (closest to the power supply). You cannot install the CPU in any other slot. When inserting the CPU into the base, align the PC board with the grooves on the top and bottom of the base. Push the CPU straight into the base until it is firmly seated in the backplane connector. Use the retaining clips to secure the CPU to the base.

WARNING: To minimize the risk of electrical shock, personal injury, or equipment damage, always disconnect the system power before installing or removing any system component.

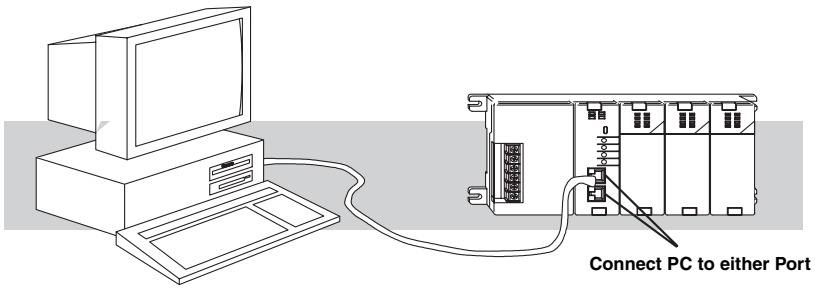


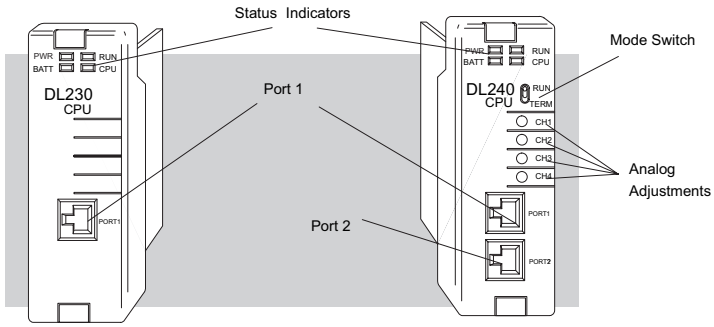
Connecting the Programming Devices

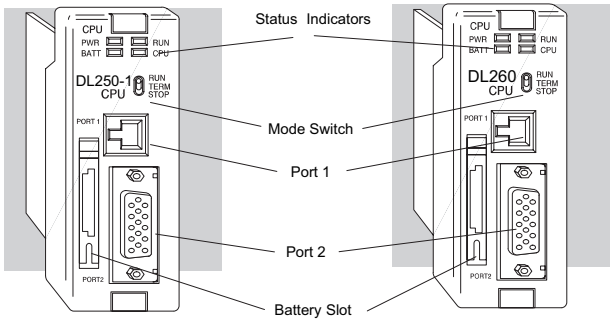
The handheld programmer is connected to the CPU with a Handheld Programmer cable. You can connect the Handheld Programmer to either port on a DL240 CPU. The Handheld Programmer is shipped with a cable. The cable is approximately 6.5 ft (200cm).



If you are using a Personal Computer with the *Direct*SOFT programming package, you can use either the top or bottom port.







CPU Setup Information

Even if you have years of experience using PLCs, there are a few tasks you need to do before you can start entering programs. This section includes some basic tasks, such as changing the CPU mode, but it also includes some tasks that you may never have to use. Here's a brief list of the items that are discussed:

- Using auxiliary functions
- Clearing the program (and other memory areas)
- How to initialize system memory
- Setting retentive memory ranges

The following paragraphs provide the setup information necessary to ready the CPU for programming, including set-up instructions for either type of programming device you are using. The D2–HPP Handheld Programmer Manual provides the Handheld keystrokes required to perform all of these operations. The ***Direct***SOFT Manual provides a description of the menus and keystrokes required to perform the setup procedures via ***Direct***SOFT.

Status Indicators

The status indicator LEDs on the CPU front panels have specific functions that can help in programming and troubleshooting.

Indicator	Status	Meaning
PWR	ON	Power good
	OFF	Power failure
RUN	ON	CPU is in Run Mode
	OFF	CPU is in Stop or Program Mode
	Blinking	CPU is in Firmware Upgrade Mode
CPU	ON	CPU self diagnostics error
	OFF	CPU self diagnostics good
BATT	ON	Low battery voltage (only with System Memory bit B7633.12 set)
	OFF	CPU battery voltage is good or disabled

Mode Switch Functions

The mode switch on the DL240, DL250–1 and DL260 CPUs provides positions for enabling and disabling program changes in the CPU. Unless the mode switch is in the TERM position, RUN and STOP mode changes will not be allowed by any interface device, (Handheld Programmer, ***Direct***SOFT programing package or operator interface). Programs may be viewed or monitored but no changes may be made. If the switch is in the TERM position and no program password is in effect, all operating modes as well as program access will be allowed through the connected programming or monitoring device.

The CPU mode can be changed in two ways:

- Use the CPU mode switch to select the operating mode.
- Place the CPU mode switch in the TERM position and use a programming device to change operating modes. In this position, you can change between Run and Program modes.

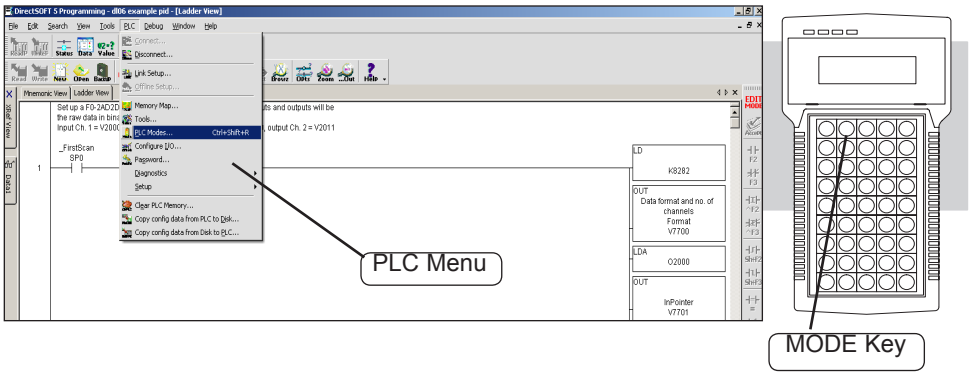
NOTE: *If the PLC is switched to the RUN Mode without a program in the CPU, the CPU will produce a FATAL ERROR which can be cleared by cycling the power to the PLC.*

Mode Switch Position	CPU Action
RUN (Run Program)	CPU is forced into the RUN mode if no errors are encountered. No changes are allowed by the attached programming/monitoring device.
TERM (Terminal)	RUN, PROGRAM and the TEST modes are available. Mode and program changes are allowed by the programming/monitoring device.
STOP (DL250–1 and DL260 only Stop Program)	CPU is forced into the STOP mode. No changes are allowed by the programming/monitoring device.

Changing Modes in the DL205 PLC

Mode Switch Position	CPU Action
RUN (Run Program)	CPU is forced into the RUN mode if no errors are encountered. No changes are allowed by the attached programming/ monitoring device.
TERM (Terminal) RUN	PROGRAM and the TEST modes are available. Mode and program changes are allowed by the programming/monitoring device.
STOP	CPU is forced into the STOP mode. No changes are allowed by the programming/monitoring device.

The CPU mode can be changed in two ways: you can use the CPU mode switch to select the operating mode, or you can place the mode switch in the TERM position and use a programming device to change operating modes. With the switch in this position, the CPU can be changed between Run and Program modes. You can use either *Direct*SOFT or the Handheld Programmer to change the CPU mode of operation. With *Direct*SOFT use the PLC menu option **PLC > Mode** or use the **Mode** button located on the Online toolbar. With the Handheld Programmer, use the MODE key.



Mode of Operation at Power Up

The DL205 CPUs will normally power up in the mode that it was in just prior to the power interruption. For example, if the CPU was in Program Mode when the power was disconnected, the CPU will power up in Program Mode (see warning note below).

WARNING: Once the super capacitor has discharged, the system memory may not retain the previous mode of operation. When this occurs, the PLC can power-up in either Run or Program Mode if the mode switch is in the term position. There is no way to determine which mode will be entered as the startup mode. Failure to adhere to this warning greatly increases the risk of unexpected equipment startup.

The mode in which the CPU will power up in is also determined by the state of System Memory bit B7633.13. If the bit is set and the Mode Switch is in the TERM position, the CPU will power-up in RUN mode. If B7633.13 is not set with the Mode Switch in TERM position, then the CPU will power up in the state it was in when it was powered down.

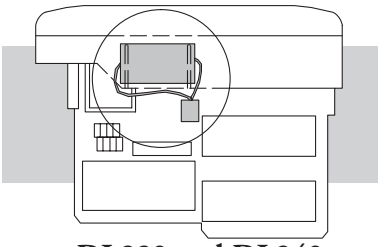
Using Battery Backup

An optional lithium battery is available to maintain the system RAM retentive memory when the DL205 system is without external power. Typical CPU battery life is five years, which includes PLC runtime and normal shut-down periods. However, consider installing a fresh battery if your battery has not been changed recently and the system will be shut down for a period of more than ten days.

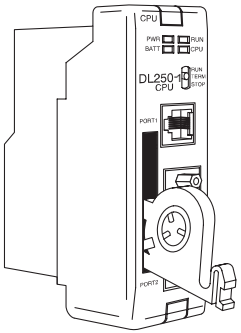
NOTE: *Before installing or replacing your CPU battery, back up your V-memory and system parameters. You can do this by using* ***Direct****SOFT to save the program, V-memory, and system parameters to hard/ floppy disk on a personal computer.*

To install the D2–BAT CPU battery in DL230 or DL240 CPUs:

1. Gently push the battery connector onto the circuit board connector.
2. Push the battery into the retaining clip. Don't use excessive force. You may break the retaining clip.
3. Make a note of the date the battery was installed.



DL230 and DL240



DL250-1 and DL260

To install the D2–BAT–1 CPU battery in the DL250–1/DL260 CPUs: (#CR2354)

1. Press the retaining clip on the battery door down and swing the battery door open.
2. Place the battery into the coin–type slot with the +, or larger, side out.
3. Close the battery door making sure that it locks securely in place.
4. Make a note of the date the battery was installed.

WARNING: Do not attempt to recharge the battery or dispose of an old battery by fire. The battery may explode or release hazardous materials.

Battery Backup

The battery backup is available immediately after the battery has been installed in the DL205 CPUs. ***The battery low (BATT) indicator will turn on if the battery is less than 2.5VDC*** (refer to the Status Indicator table on page 3-12). Special Relay 43 (SP43) will also be activated. The low battery indication is enabled by setting bit 12 of V7633 (B7633.12). If the low-battery feature is not desired, do not set bit V7633.12.

The super capacitor will retain memory IF it is configured as retentive regardless of the state of B7633.12. The battery will be the same, but for a much longer time.

Auxiliary Functions

Many CPU set-up tasks involve the use of Auxiliary (AUX) Functions. The AUX Functions perform many different operations, including clearing ladder memory, displaying the scan time, copying programs to EEPROM in the Handheld Programmer, etc. They are divided into categories that affect different system parameters. Appendix A provides a description of the AUX functions.

You can access the AUX Functions from *Direct*SOFT or from the DL205 Handheld Programmer. The manuals for those products provide step-by-step procedures for accessing the AUX Functions. Some of these AUX Functions are designed specifically for the Handheld Programmer setup, so they will not be needed (or available) with the *Direct*SOFT package. The following table shows a list of the Auxiliary functions for the different CPUs and the Handheld Programmer.

NOTE: *The Handheld Programmer may have additional AUX functions that are not supported with the DL205 CPUs.*

AUX Function and Description		230	240	250–1	260
AUX 2* — RLL Operations					
21	Check Program	✓	✓	✓	✓
22	Change Reference	✓	✓	✓	✓
23	Clear Ladder Range	✓	✓	✓	✓
24	Clear All Ladders	✓	✓	✓	✓
AUX 3* — V-Memory Operations					
31	Clear V Memory	✓	✓	✓	✓
AUX 4* — I/O Configuration					
41	Show I/O Configuration	✓	✓	✓	✓
42	I/O Diagnostics	✓	✓	✓	✓
44	Power-up I/O Configuration Check	✓	✓	✓	✓
45	Select Configuration	✓	✓	✓	✓
46	Configure I/O	X	X	✓	✓
AUX 5* — CPU Configuration					
51	Modify Program Name	✓	✓	✓	✓
52	Display / Change Calendar	X	✓	✓	✓
53	Display Scan Time	✓	✓	✓	✓
54	Initialize Scratchpad	✓	✓	✓	✓
55	Set Watchdog Timer	✓	✓	✓	✓
56	Set CPU Network Address	X	✓	✓	✓
57	Set Retentive Ranges	✓	✓	✓	✓
58	Test Operations	✓	✓	✓	✓
59	Bit Override	X	✓	✓	✓
5B	Counter Interface Config.	✓	✓	✓	✓
5C	Display Error History	X	✓	✓	✓

AUX Function and Description		230	240	250–1	260	HPP
AUX 6* — Handheld Programmer Configuration						
61	Show Revision Numbers	✓	✓	✓	✓	–
62	Beeper On / Off	X	X	X	X	✓
65	Run Self Diagnostics	X	X	X	X	✓
AUX 7* — EEPROM Operations						
71	Copy CPU memory to HPP EEPROM	X	X	X	X	✓
72	Write HPP EEPROM to CPU	X	X	X	X	✓
73	Compare CPU to HPP EEPROM	X	X	X	X	✓
74	Blank Check (HPP EEPROM)	X	X	X	X	✓
75	Erase HPP EEPROM	X	X	X	X	✓
76	Show EEPROM Type (CPU and HPP)	X	X	X	X	✓
AUX 8* — Password Operations						
81	Modify Password	✓	✓	✓	✓	–
82	Unlock CPU	✓	✓	✓	✓	–
83	Lock CPU	✓	✓	✓	✓	–

✓ *Supported*
X *Not Supported*
\- *Not Applicable*

Clearing an Existing Program

Before you enter a new program, you should always clear ladder memory. You can use AUX Function 24 to clear the complete program.

You can also use other AUX functions to clear other memory areas.

AUX 23 — Clear Ladder Range

AUX 24 — Clear all Ladders

AUX 31 — Clear V-Memory

Initializing System Memory

The DL205 CPUs maintain system parameters in a memory area often referred to as the "scratchpad." In some cases, you may make changes to the system setup that will be stored in system memory. For example, if you specify a range of Control Relays (CRs) as retentive, these changes are stored. AUX 54 resets the system memory to the default values.

WARNING: You may never have to use this feature unless you want to clear any set-up information that is stored in system memory. Usually, you will only need to initialize the system memory if you are changing programs and the old program required a special system setup. You can usually change from program to program without ever initializing system memory. Remember, this AUX function will reset all system memory. If you have set special parameters such as retentive ranges, etc., they will be erased when AUX 54 is used. Make sure that you have considered all ramifications of this operation before you select it.

Setting the Clock and Calendar

☒ 230
☑ 240
☑ 250-1
☑ 260

The DL240, DL250–1 and DL260 also have a Clock/Calendar that can be used for many purposes. If you need to use this feature, AUX functions are available that allow you to set the date and time. For example, you would use AUX 52, Display/Change Calendar to set the time and date with the Handheld Programmer. With *Direct*SOFT you would use the PLC set-up menu options using K–Sequence protocol only.

The CPU uses the following format to display the date and time.

- Date — Year, Month, Date, Day of week (0 – 6, Sunday through Saturday)
- Time — 24-hour format, Hours, Minutes, Seconds

Handheld Programmer Display

```
23:08:17  08/02/20
```

You can use the AUX function to change any component of the date or time. However, the CPU will not automatically correct any discrepancy between the date and the day of the week. For example, if you change the date to the 15th of the month and the 15th is on a Thursday, you will also have to change the day of the week (unless the CPU already shows the date as Thursday). The day of the week can only be set using the Handheld Programmer.

Setting the CPU Network Address

☒ 230
☑ 240
☑ 250-1
☑ 260

The DL240, DL250–1 and DL260 CPUs have built in *Direct*Net ports. You can use the Handheld Programmer to set the network address for the port and the port communication parameters. The default settings are:

- Station Address 1
- Hex Mode
- Odd Parity
- 9600 Baud

The *Direct*Net Manual provides additional information about choosing the communication settings for network operation.

Setting Retentive Memory Ranges

The DL205 CPUs provide certain ranges of retentive memory by default. The default ranges are suitable for many applications, but you can change them if your application requires additional retentive ranges or no retentive ranges at all. The default settings are:

Memory Area	DL230		DL240		DL250–1		DL260	
	Default Range	Avail. Range	Default Range	Avail. Range	Default Range	Avail. Range	Default Range	Avail. Range
Control Relays	C300 – C377	C0 – C377	C300 – C377	C0 – C377	C1000 – C1777	C0 – C1777	C1000 – C3777	C0 – C3777
V-Memory	V2000 – V7777	V0 – V7777	V2000 – V7777	V0 – V7777	V1400 – V3777	V0 – V17777	V400 – V37777	V0 – V37777
Timers	None by default	T0 – T77	None by default	T0 – T177	None by default	T0 – T377	None by default	T0 – T377
Counters	CT0 – CT77	CT0 – CT77	CT0 – CT177	CT0 – CT177	CT0 – CT177	CT0 – CT177	CT0 – CT377	CT0 – CT377
Stages	None by default	S0 – S377	None by default	S0 – S777	None by default	S0 – S1777	None by default	S0 – S1777

You can use AUX 57 to set the retentive ranges. You can also use *Direct*SOFT menus to select the retentive ranges.

WARNING: The DL205 CPUs do not come with a battery. The super capacitor will retain the values in the event of a power loss, but only for a short period of time, depending on conditions. If the retentive ranges are important for your application, make sure you obtain the optional battery.

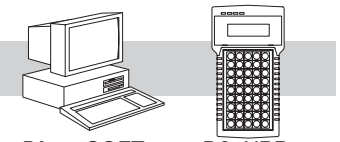
Using a Password

The DL205 CPUs allow you to use a password to help minimize the risk of unauthorized program and/or data changes. Once you enter a password you can "lock" the CPU against access. Once the CPU is locked you must enter the password before you can use a programming device to change any system parameters.

You can select an 8-digit numeric password. The CPUs are shipped from the factory with a password of 00000000. All zeros removes the password protection. If a password has been entered into the CPU, you cannot enter all zeros to remove it. Once you enter the correct password, you can change the password to all zeros to remove the password protection. For more information on passwords, see the appropriate appendix on auxiliary functions.

WARNING: Make sure you remember your password. If you forget your password you will not be able to access the CPU. The CPU must be returned to the factory to have the password (along with the ladder project) removed. It is the policy of AutomationDirect to require the memory of the PLC to be cleared along with the password.

You can use the D2–HPP Handheld Programmer or *Direct*SOFT to enter a password. The following diagram shows how you can enter a password with the Handheld Programmer.



Select AUX 81

CLR CLR I 8 B 1 AUX ENT

PASSWORD
00000000

Enter the new 8-digit password

X X • • • X ENT

PASSWORD
XXXXXXXX

Press CLR to clear the display

The CPU can be locked three ways once the password has been entered.

- If the CPU power is disconnected, the CPU will be automatically locked against access.
- If you enter the password with *Direct*SOFT, the CPU will be automatically locked against access when you exit *Direct*SOFT.
- Use AUX 83 to lock the CPU.

When you use *Direct*SOFT, you will be prompted for a password if the CPU has been locked. If you use the Handheld Programmer, you have to use AUX 82 to unlock the CPU. Once you enter AUX 82, you will be prompted to enter the password.

***NOTE**: The DL240, DL250–1 and DL260 CPUs offer multi–level passwords for even more password protection of the ladder program. This allows password protection while not locking the communication port to an operator interface. The multi-level password can be invoked by creating a password with an upper case "A" followed by seven numeric characters (e.g., A1234567).*

Setting the Analog Potentiometer Ranges

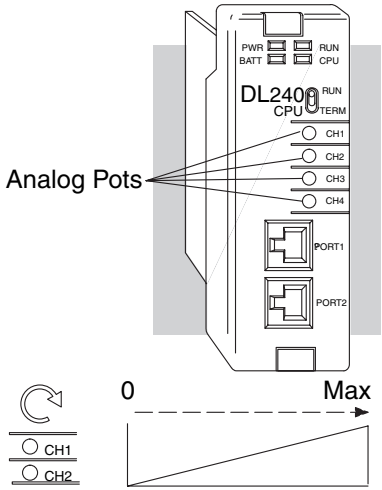
☒ 230
☑ 240
☒ 250-1
☒ 260

Four analog potentiometers (pots) are on the face plate of the DL240 CPU. These pots can be used to change timer constants, frequency of pulse train output, value for an analog output module, etc.

Each analog channel has corresponding V-memory locations for setting lower and upper limits for each analog channel.

To increase the value associated with the analog pot, turn the pot clockwise. To decrease the value, turn the pot counter clockwise

Turn clockwise to increase value.



The table below shows the V-memory locations used for each analog channel. These are the default locations for the analog pots.

	CH1	CH2	CH3	CH4
Analog Data	V3774	V3775	V3776	V3777
Analog Data Lower Limit	V7640	V7642	V7644	V7646
Analog Data Upper Limit	V7641	V7643	V7645	V7647

You can use the program logic to load the limits into these locations, or, you can use a programming device to load the values. The range for each limit is 0 – 9999.

These analog pots have a resolution of 256 pieces. Therefore, if the span between the upper and lower limits is less than or equal to 256, then you have better resolution or, more precise control.

Use the formula shown to determine the smallest amount of change that can be detected.

For example, a range of 100 – 600 would result in a resolution of 1.95. Therefore, the smallest increment would be 1.95 units. (The actual result depends on exactly how you are using the values in the control program).

$$\text{Resolution} = \frac{H - L}{256}$$

H = high limit of the range
L = low limit of the range

Example Calculations:

H = 600
L = 100

$$\text{Resolution} = \frac{600-100}{256}$$

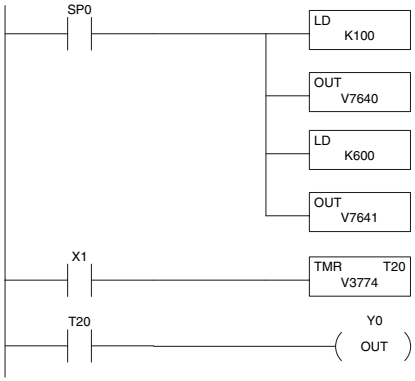
$$\text{Resolution} = \frac{500}{256}$$

$$\text{Resolution} = 1.95$$

The following example shows how you could use these analog potentiometers to change the preset value for a timer. See Chapter 5 for details on how these instructions operate.

Program loads ranges into V-memory

*Direct*SOFT

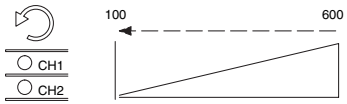


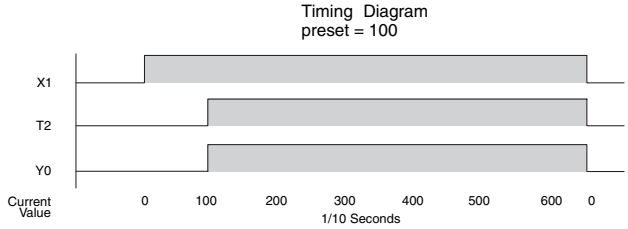
Load the lower limit (100) for the analog range on Ch1 into V7640.

Load the upper limit (600) for the analog range on Ch1 into V7641.

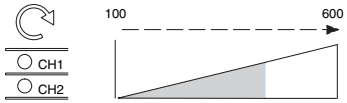
Use V3774 as the preset for the timer. This will allow you to quickly adjust the preset from 100 to 600 with the CH1 analog pot.

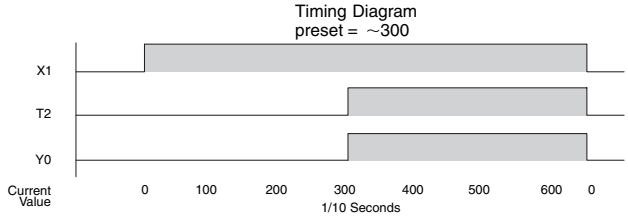
Turn all the way counter-clockwise to use lowest value





Turn clockwise to increase the timer preset.

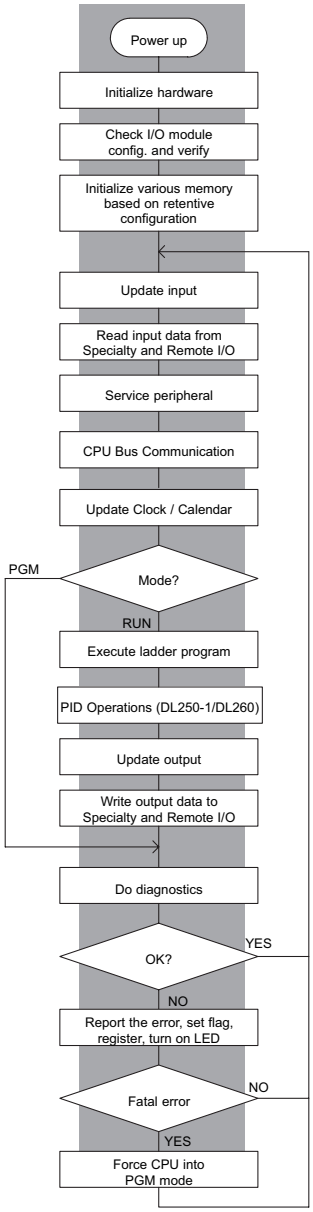




CPU Operation

Achieving the proper control for your equipment or process requires a good understanding of how DL205 CPUs control all aspects of system operation. The flowchart below shows the main tasks of the CPU operating system. In this section, we will investigate four aspects of CPU operation:

- CPU Operating System — The CPU manages all aspects of system control.
- CPU Operating Modes — The three primary modes of operation are Program Mode, Run Mode, and Test Mode.
- CPU Timing — The two important areas we discuss are the I/O response time and the CPU scan time.
- CPU Memory Map — The CPU's memory map shows the CPU addresses of various system resources, such as timers, counters, inputs, and outputs.



CPU Operating System

At power up, the CPU initializes the internal electronic hardware. Memory initialization starts with examining the retentive memory settings. In general, the contents of retentive memory are preserved, and non-retentive memory is initialized to zero (unless otherwise specified).

After the one-time power-up tasks, the CPU begins the cyclical scan activity. The flowchart to the right shows how the tasks differ based on the CPU mode and the existence of any errors. The "scan time" is defined as the average time around the task loop. Note that the CPU is always reading the inputs, even during program mode. This allows programming tools to monitor input status at any time.

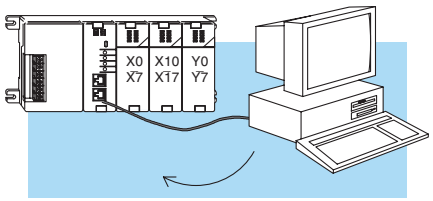
The outputs are only updated in Run mode. In Program mode, they are in the off state.

In Run Mode, the CPU executes the user ladder program. Immediately afterwards, any PID loops which are configured are executed (DL250-1 and DL260). Then the CPU writes the output results of these two tasks to the appropriate output points.

Error detection has two levels: Non-fatal and fatal. Non-fatal errors are reported, but the CPU remains in its current mode. If a fatal error occurs, the CPU is forced into program mode and the outputs go off.

Program Mode Operation

In Program Mode the CPU does not execute the application program or update the output modules. The primary use for Program Mode is to enter or change an application program. You also use the program mode to set up CPU parameters, such as the network address, retentive memory areas, etc.



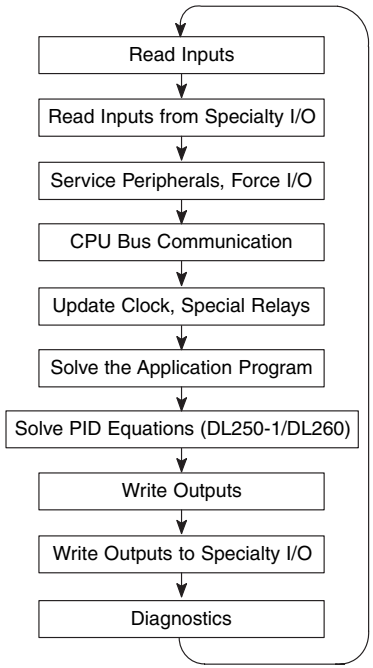
Download Program

You can use the mode switch on the DL250–1 and DL260 CPUs to select Program Mode operation. Or, with the switch in TERM position, you can use a programming device such as the Handheld Programmer to place the CPU in Program Mode.

Run Mode Operation

In Run Mode, the CPU executes the application program, does PID calculations for configured PID loops (DL250-1/DL260), and updates the I/O system. You can perform many operations during Run Mode. Some of these include:

- Monitor and change I/O point status
- Update timer/counter preset values
- Update Variable memory locations



Run Mode operation can be divided into several key areas. It is very important you understand how each of these areas of execution can affect the results of your application program solutions.

You can use the mode switch to select Run Mode operation (DL240, DL250–1 and DL260). Or, with the mode switch in TERM position, you can use a programming device, such as the Handheld Programmer, to place the CPU in Run Mode.

You can also edit the program during Run Mode. The Run Mode Edits are not "bumpless." Instead, the CPU maintains the outputs in their last state while it accepts the new program information. If an error is found in the new program, then the CPU will turn all the outputs off and enter the Program Mode.

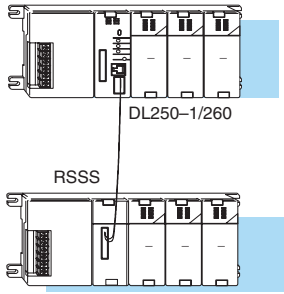
WARNING: Only authorized personnel fully familiar with all aspects of the application should make changes to the program. Changes during Run Mode become effective immediately. Make sure you thoroughly consider the impact of any changes to minimize the risk of personal injury or damage to equipment.

Read Inputs

The CPU reads the status of all inputs, then stores it in the image register. Input image register locations are designated with an X followed by a memory location. Image register data is used by the CPU when it solves the application program. Of course, an input may change after the CPU has read the inputs. Generally, the CPU scan time is measured in milliseconds. If you have an application that cannot wait until the next I/O update, you can use Immediate Instructions. These do not use the status of the input image register to solve the application program. The Immediate instructions immediately read the input status directly from I/O modules. However, this lengthens the program scan since the CPU has to read the I/O point status again. A complete list of the Immediate instructions is included in Chapter 5.

Read Inputs from Specialty and Remote I/O

After the CPU reads the inputs from the input modules, it reads any input point data from any Specialty modules that are installed, such as Counter Interface modules, etc. This is also the portion of the scan that reads the input status from Remote I/O bases.



***NOTE**: It may appear the Remote I/O point status is updated every scan. This is not quite true. The CPU will receive information from the Remote I/O Master module every scan, but the Remote Master may not have received an update from all the Remote Slaves. Remember, the Remote I/O link is managed by the Remote Master, not the CPU.*

Service Peripherals and Force I/O

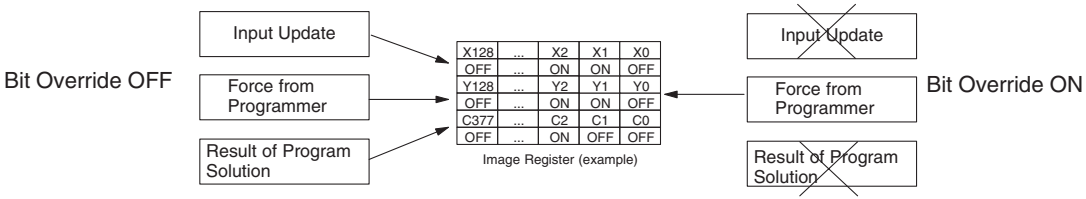
After the CPU reads the inputs from the input modules, it reads any attached peripheral devices. This is primarily a communications service for any attached devices. For example, it would read a programming device to see if any input, output, or other memory type status needs to be modified. Two basic types of forcing are available with the DL205 CPUs.

***NOTE**: **Direct**Net protocol does not support bit operations.*

- Forcing from a peripheral – not a permanent force, good only for one scan
- Bit Override (DL240, DL250–1 and DL260) – holds the I/O point (or other bit) in the current state. Valid bits are X, Y, C, T, CT, and S. These memory types are discussed in more detail later in this chapter.

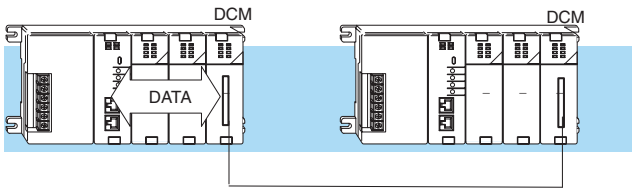
Regular Forcing — This type of forcing can temporarily change the status of a discrete bit. For example, you may want to force an input on, even though it is really off. This allows you to change the point status that was stored in the image register. This value will be valid until the image register location is written to during the next scan. This is primarily useful during testing situations when you need to force a bit on to trigger another event.

Bit Override — (DL240, DL250–1 and DL260) Bit override can be enabled on a point-by-point basis by using AUX 59 from the Handheld Programmer or, by a menu option from within *Direct*SOFT. Bit override basically disables any changes to the discrete point by the CPU. For example, if you enable bit override for X1, and X1 is off at the time, then the CPU will not change the state of X1. This means that even if X1 comes on, the CPU will not acknowledge the change. So, if you used X1 in the program, it would always be evaluated as "off" in this case. Of course, if X1 was on when the bit override was enabled, then X1 would always be evaluated as "on." There is an advantage available when you use the bit override feature. The regular forcing is not disabled because the bit override is enabled. For example, if you enabled the Bit Override for Y0 and it was off at the time, then the CPU would not change the state of Y0. However, you can still use a programming device to change the status. Now, if you use the programming device to force Y0 on, it will remain on and the CPU will not change the state of Y0. If you then force Y0 off, the CPU will maintain Y0 as off. The CPU will never update the point with the results from the application program or from the I/O update until the bit override is removed. The following diagram shows a brief overview of the bit override feature. Notice the CPU does not update the Image Register when bit override is enabled



CPU Bus Communication

Specialty Modules, such as the Data Communications Module, can transfer data to and from the CPU over the CPU bus on the backplane. This data is more than standard I/O point status. This type of communications can only occur on the CPU (local) base. A portion of the execution cycle is used to communicate with these modules. The CPU performs both read and write requests during this segment.



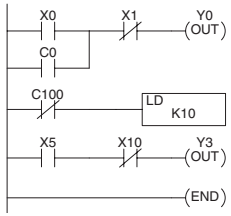
Update Clock, Special Relays and Special Registers

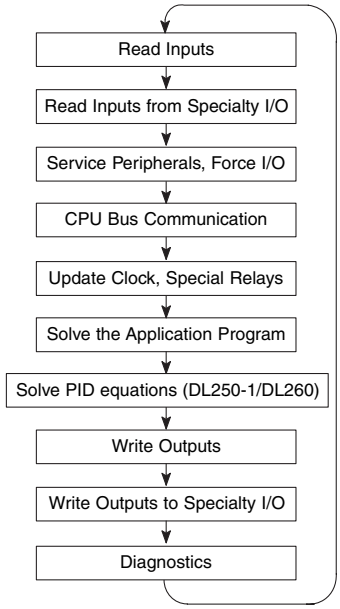
The DL240 , DL250–1 and DL260 CPUs have an internal real-time clock and calendar timer which are accessible to the application program. Special V-memory locations hold this information. This portion of the execution cycle makes sure these locations get updated on every scan. Several different Special Relays, such as diagnostic relays, etc., are also updated during this segment.

Solve Application Program

The CPU evaluates each instruction in the application program during this segment of the scan cycle. The instructions define the relationship between input conditions and the system outputs.

The CPU begins with the first rung of the ladder program, evaluating it from left to right and from top to bottom. It continues, rung by rung, until it encounters the END coil instruction. At that point, a new image for the outputs is complete.





The internal control relays (C), the stages (S), and the variable memory (V) are also updated in this segment.

You may recall the CPU may have obtained and stored forcing information when it serviced the peripheral devices. If any I/O points or memory data have been forced, the output image register also contains this information.

***NOTE**: If an output point was used in the application program, the results of the program solution will overwrite any forcing information that was stored. For example, if Y0 was forced on by the programming device, and a rung containing Y0 was evaluated such that Y0 should be turned off, then the output image register will show that Y0 should be off. Of course, you can force output points that are not used in the application program. In this case, the point remains forced because there is no solution that results from the application program execution.*

Solve PID Loop Equations

☒ 230
☒ 240
☑ 250-1
☑ 260

The DL260 CPU can process up to 16 PID loops and the DL250–1 can process up to 4 PID loops. The loop calculations are run as a separate task from the ladder program execution, immediately following it. Only loops that have been configured are calculated, and then only according to a built-in loop scheduler. The sample time (calculation interval) of each loop is programmable. Please refer to Chapter 8, PID Loop Operation, for more on the effects of PID loop calculation on the overall CPU scan time.

Write Outputs

Once the application program has solved the instruction logic and constructed the output image register, the CPU writes the contents of the output image register to the corresponding output points located in the local CPU base or the local expansion bases. Remember, the CPU also made sure any forcing operation changes were stored in the output image register, so the forced points get updated with the status specified earlier.

Write Outputs to Specialty and Remote I/O

After the CPU updates the outputs in the local and expansion bases, it sends the output point information that is required by any Specialty modules that are installed. For example, this is the portion of the scan that writes the output status from the image register to the Remote I/O racks.

***NOTE**: It may appear the Remote I/O point status is updated every scan. This is not quite true. The CPU will send the information to the Remote I/O Master module every scan, but the Remote Master will update the actual remote modules during the next communication sequence between the master and slave modules. Remember, the Remote I/O link communication is managed by the Remote Master, not the CPU.*

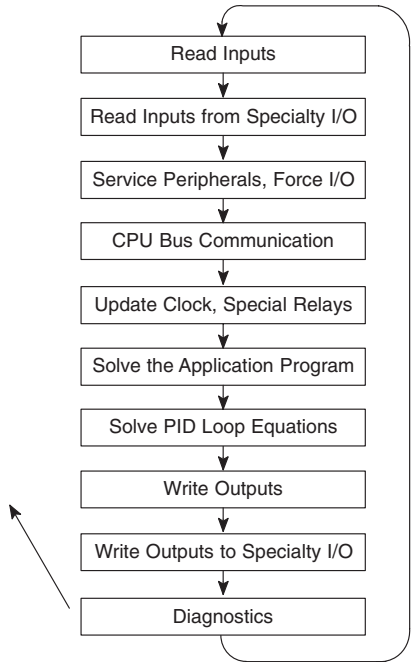
Diagnostics

During this part of the scan, the CPU performs all system diagnostics and other tasks, such as:

- calculating the scan time
- updating special relays
- resetting the watchdog timer

DL205 CPUs automatically detect and report many different error conditions. Appendix B contains a listing of the various error codes available with the DL205 system.

One of the more important diagnostic tasks is the scan time calculation and watchdog timer control. DL205 CPUs have a "watchdog" timer that stores the maximum time allowed for the CPU to complete the solve application segment of the scan cycle. The default value set from the factory is 200ms. If this time is exceeded the CPU will enter the Program Mode, turn off all outputs, and report the error. For example, the Handheld Programmer displays "E003 S/W TIMEOUT" when the scan overrun occurs.



You can use AUX 53 to view the minimum, maximum, and current scan time. Use AUX 55 to increase or decrease the watchdog timer value. There is also an RSTWT instruction that can be used in the application program to reset the watch dog timer during the CPU scan.

I/O Response Time

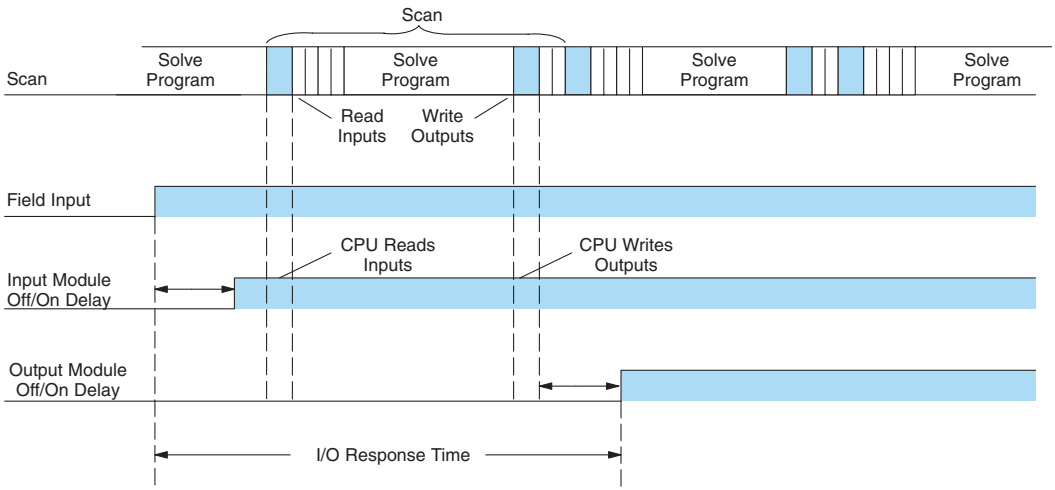
Is Timing Important for Your Application?

I/O response time is the amount of time required for the control system to sense a change in an input point and update a corresponding output point. In the majority of applications, the CPU performs this task practically instantaneously. However, some applications do require extremely fast update times. Four things can affect the I/O response time:

- The point in the scan period when the field input changes states
- Input module Off to On delay time
- CPU scan time
- Output module Off to On delay time

Normal Minimum I/O Response

The I/O response time is shortest when the module senses the input change before the Read Inputs portion of the execution cycle. In this case the input status is read, the application program is solved, and the output point gets updated. The following diagram shows an example of the timing for this situation.



In this case, you can calculate the response time by simply adding the following items:

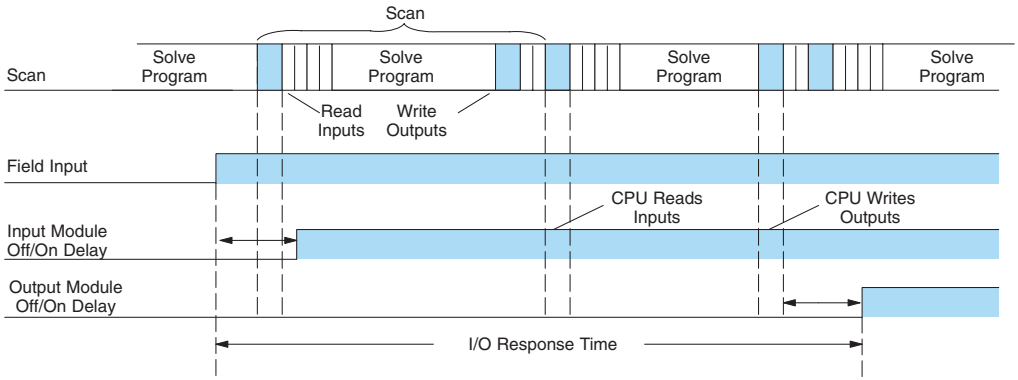
Input Delay + Scan Time + Output Delay = Response Time

Normal Maximum I/O Response

The I/O response time is longest when the module senses the input change after the Read Inputs portion of the execution cycle. In this case the new input status does not get read until the following scan. The following diagram shows an example of the timing for this situation.

In this case, you can calculate the response time by simply adding the following items:

Input Delay +(2 x Scan Time) + Output Delay = Response Time

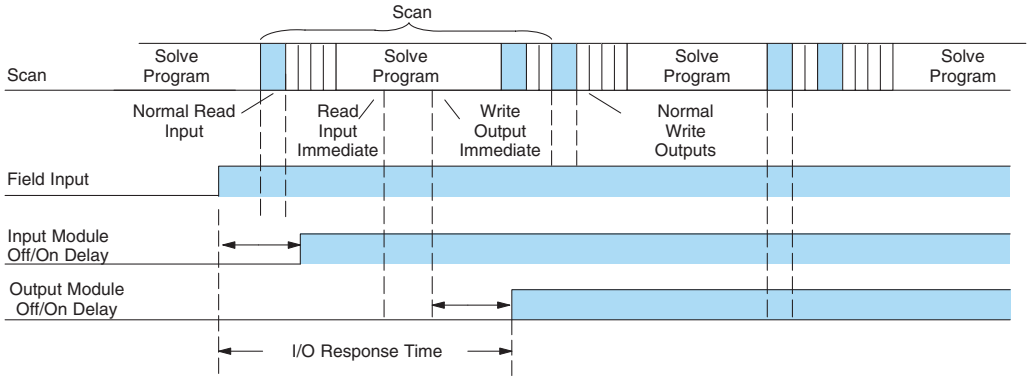


Improving Response Time

You can do a few things to help improve throughput.

- Choose instructions with faster execution times
- Use immediate I/O instructions (which update the I/O points during the ladder program execution segment)
- Choose modules that have faster response times

Immediate I/O instructions are probably the most useful technique. The following example shows immediate input and output instructions and their effect.



In this case, you can calculate the response time by simply adding the following items:

Input Delay + Instruction Execution Time + Output Delay = Response Time

The instruction execution time is calculated by adding the time for the immediate input instruction, the immediate output instruction, and all instructions in between.

***NOTE**: When the immediate instruction reads the current status from a module, it uses the results to solve that one instruction without updating the image register. Therefore, any regular instructions that follow will still use image register values. Any immediate instructions that follow will access the module again to update the status.*

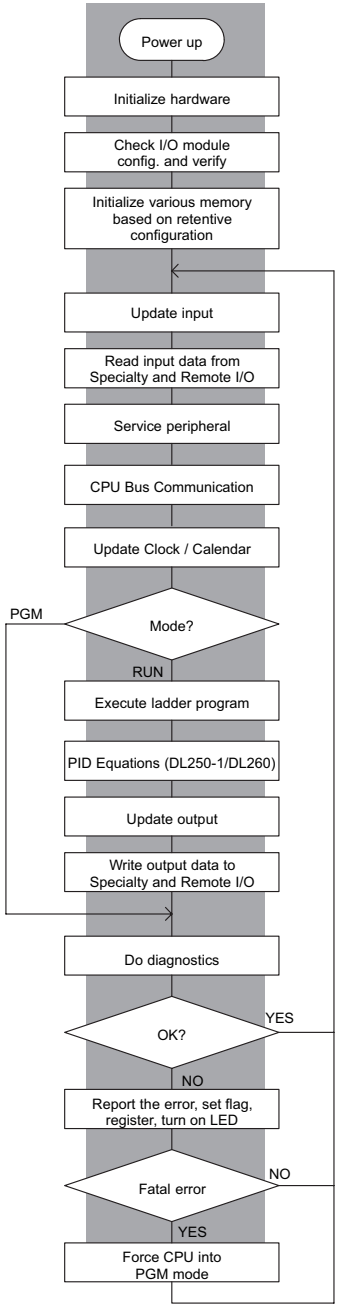
CPU Scan Time Considerations

The scan time covers all the cyclical tasks that the operating system performs. You can use *Direct*SOFT or the Handheld Programmer to display the minimum, maximum, and current scan times that have occurred since the previous Program Mode to Run Mode transition. This information can be very important when evaluating system performance.

As shown previously, there are several segments that make up the scan cycle. Each of these segments requires a certain amount of time to complete. Of all the segments, the only one you really have the most control over is the amount of time it takes to execute the application program. This is because different instructions take different amounts of time to execute. So, if you think you need a faster scan, then you can try to choose faster instructions.

Your choice of I/O modules and system configuration, such as expansion or remote I/O, can also affect the scan time; however, the application usually dictates them.

For example, if you need to count pulses at high rates of speed, then you will probably have to use a High-Speed Counter module. Also, if you have I/O points that need to be located several hundred feet from the CPU, then you need remote I/O because it is much faster and cheaper to install a single remote I/O cable than it is to run all those signal wires for each individual I/O point. The following paragraphs provide some general information on how much time some of the segments can require.



Initialization Process

The CPU performs an initialization task once the system power is on. The initialization task is performed once at power up, so it does not affect the scan time for the application program.

Reading Inputs

Initialization	DL230	DL240	DL250–1	DL260
Minimum Time	1.6 Seconds	1.0 Seconds	1.2 Seconds	1.2 Seconds
Maximum Time	3.6 Seconds	2.0 Seconds	2.7 Seconds(w/ 2 exp. bases)	3.7 Seconds (w/ 4 exp. bases)

The time required to read the input status for the input modules depends on which CPU you are using and the number of input points in the base. The following table shows typical update times required by the CPU.

For example, the time required for a DL240 to read two 8-point input modules would be

Timing Factors	DL230	DL240	DL250–1	DL260
Overhead	64.0 µs	32.0 µs	12.6 µs	12.6 µs
Per input point	6.0 µs	12.3 µs	2.5 µs	2.5 µs

calculated as follows, where NI is the total number of input points:

Formula

Time = 32µs + (12.3 x NI)

Example

Time = 32µs + (12.3 x 16)

Time = 228.8 µs

***NOTE**: This information provides the amount of time the CPU spends reading the input status from the modules. Don't confuse this with the I/O response time that was discussed earlier.*

Reading Inputs from Specialty I/O

During this portion of the cycle the CPU reads any input points associated with the following:

- Remote I/O
- Specialty Modules (such as High-Speed Counter, etc)

The time required to read any input status from these modules depends on which CPU you are using, the number of modules, and the number of input points.

Remote Module	DL230	DL240	DL250–1	DL260
Overhead	N/A	6.0 µs	1.82 µs	1.82 µs
Per module (with inputs)	N/A	67.0 µs	17.9 µs	17.9 µs
Per input point	N/A	40.0 µs	2.0 µs	2.0 µs

For example, the time required for a DL240 to read two 8-point input modules (located in a Remote base) would be calculated as follows, where NM is the number of modules and NI is the total number of input points:

Remote I/O

Formula

Time = 6µs + (67µs x NM) + (40µs x NI)

Example

Time = 6µs + (67µs x 2) + (40µs x 16)

Time = 780µs

Service Peripherals

Communication requests can occur at any time during the scan, but the CPU only "logs" the requests for service until the Service Peripherals portion of the scan. The CPU does not spend any time on this if there are no peripherals connected.

To Log Request (anytime)		DL230	DL240	DL250–1	DL260
Nothing Connected	Min. & Max.	0 µs	0 µs	0 µs	0 µs
Port 1	Send Min. / Max.	22/28 µs	23/26 µs	3.2/9.2 µs	3.2/9.2 µs
	Rec. Min. / Max.	24/58 µs	52/70 µs	25.0/35.0 µs	25.0/35.0 µs
Port 2	Send Min. / Max.	N/A	26/30 µs	3.6/11.5 µs	3.6/11.5 µs
	Rec. Min. / Max.	N/A	60/75 µs	35.0/44.0 µs	35.0/44.0 µs

During the Service Peripherals portion of the scan, the CPU analyzes the communications request and responds as appropriate. The amount of time required to service the peripherals depends on the content of the request.

To Service Request	DL230	DL240	DL250–1	DL260
Minimum	260µs	250µs	8µs	8µs
Run Mode Max.	30ms	20ms	410µs	410µs
Program Mode Max.	3.5 Seconds	4 Seconds	2 Seconds	3.7 Seconds

CPU Bus Communication

Some specialty modules can also communicate directly with the CPU via the CPU bus. During this portion of the cycle the CPU completes any CPU bus communications. The actual time required depends on the type of modules installed and the type of request being processed.

***NOTE**: Some specialty modules can have a considerable impact on the CPU scan time. If timing is critical in your application, consult the module documentation for any information concerning the impact on the scan time.*

Update Clock/Calendar, Special Relays, Special Registers

The clock, calendar, and special relays are updated and loaded into special V-memory locations during this time. This update is performed during both Run and Program Modes.

Modes		DL230	DL240	DL250–1	DL260
Program Mode	Minimum	8.0 µs fixed	35.0 µs	11.0 µs	11.0 µs
	Maximum	8.0 µs fixed	48.0 µs	11.0 µs	11.0 µs
Run Mode	Minimum	20.0 µs	60.0 µs	19.0 µs	19.0 µs
	Maximum	26.0 µs	85.0 µs	26.0 µs	26.0 µs

Writing Outputs

The time required to write the output status for the local and expansion I/O modules depends on which CPU you are using and the number of output points in the base. The following table shows typical update times required by the CPU.

Timing Factors	DL230	DL240	DL250–1	DL260
Overhead	66.0 µs	33.0 µs	28.1 µs	28.1 µs
Per output point	8.5 µs	14.6 µs	3.0 µs	3.0 µs

For example, the time required for a DL240 to write data for two 8-point output modules would be calculated as follows (where NO is the total number of output points):

Formula

Time = 33 + (NO x 14.6 µs)

Example

Time = 33 + (16 x 14.6 µs)

Time = 266.6 µs

Writing Outputs to Specialty I/O

During this portion of the cycle the CPU writes any output points associated with the following.

- Remote I/O
- Specialty Modules (such as High-Speed Counter, etc)

The time required to write any output image register data to these modules depends on which CPU you are using, the number of modules, and the number of output points.

Remote Module	DL230	DL240	DL250–1	DL260
Overhead	N/A	6.0 µs	1.9 µs	1.9 µs
Per module (with outputs)	N/A	67.5 µs	17.7 µs	17.7 µs
Per output point	N/A	46.0 µs	3.2 µs	3.2 µs

For example, the time required for a DL240 to write two 8-point output modules (located in a Remote base) would be calculated as follows, where NM is the number of modules and NO is the total number of output points:

Remote I/O

Formula

Time = 6µs + (67.5 µs x NM) + (46µs x NO)

Example

Time = 6µs + (67.5 µs x 2) + (46µs x 16)

Time = 877µs

***NOTE**: This total time is the actual time required for the CPU to update these outputs. This does not include any additional time that is required for the CPU to actually service the particular specialty modules.*

Diagnostics

The DL205 CPUs perform many types of system diagnostics. The amount of time required depends on many things, such as the number of I/O modules installed, etc. The following table shows the minimum and maximum times that can be expected.

Diagnostic Time	DL230	DL240	DL250–1	DL260
Minimum	600.0 µs	422.0 µs	26.8 µs	26.8 µs
Maximum	900.0 µs	855.0 µs	103.0 µs	103.0 µs

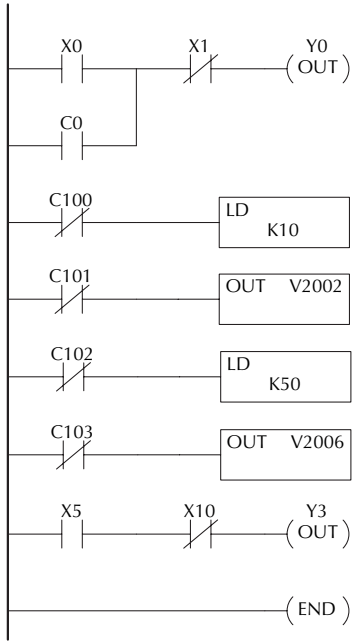
Application Program Execution

The CPU processes the program from the top (address 0) to the END instruction. The CPU executes the program left to right and top to bottom. As each rung is evaluated, the appropriate image register or memory location is updated.

The time required to solve the application program depends on the type and number of instructions used and the amount of execution overhead.

You can add the execution times for all the instructions in your program to find the total program execution time. For example, the execution time for a DL240 running the program shown would be calculated as follows:

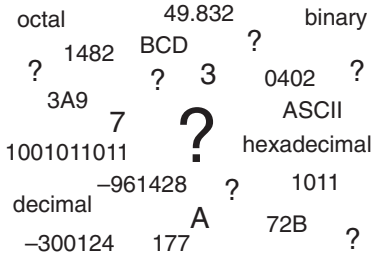
Instruction	Time
STR X0	1.4µs
OR C0	1.0µs
ANDN X1	1.2µs
OUT Y0	7.95µs
STRN C100	1.6µs
LD K10	62.0µs
STRN C101	1.6µs
OUT V2002	21.0µs
STRN C102	1.6µs
LD K50	62.0µs
STRN C103	1.6µs
OUT V2006	21.0µs
STR X5	1.4µs
ANDN X10	1.2µs
OUT Y3	7.95µs
END	16.0µs
TOTAL	210.5µs



Appendix C provides a complete list of instruction execution times for DL205 CPUs.

Program Control Instructions — the DL240, DL250–1 and DL260 CPUs offer additional instructions that can change the way the program executes. These instructions include FOR/NEXT loops, Subroutines, and Interrupt Routines. These instructions can interrupt the normal program flow and affect the program execution time. Chapter 5 provides detailed information on how these different types of instructions operate.

PLC Numbering Systems



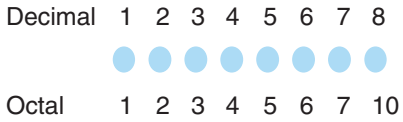
If you are a new PLC user or are using *Direct*LOGIC PLCs for the first time, please take a moment to study how our PLCs use numbers. You'll find that each PLC manufacturer has its own conventions on the use of numbers in their PLCs. Take a moment to familiarize yourself with how numbers are used in *Direct*LOGIC PLCs. The information you learn here applies to all our PLCs.

As any good computer does, PLCs store and manipulate numbers in binary form: ones and zeros. So why do we have to deal with numbers in so many different forms? Numbers have meaning, and some representations are more convenient than others for particular purposes. Sometimes we use numbers to represent a size or amount of something. Other numbers refer to locations or addresses, or to time. In science we attach engineering units to numbers to give a particular meaning (see Appendix H for numbering system details).

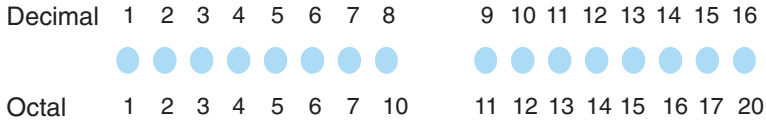
PLC Resources

PLCs offer a fixed number of resources, depending on the model and configuration. We use the word "resources" to include variable memory (V-memory), I/O points, timers, counters, etc. Most modular PLCs allow you to add I/O points in groups of eight. In fact, all the resources of our PLCs are counted in octal. It's easier for computers to count in groups of eight than ten, because eight is an even power of two.

Octal means simply counting in groups of eight. In the figure to the right, there are eight circles. The quantity in decimal is "8," but in octal it is "10" (8 and 9 are not valid in octal). In octal, "10" means 1 group of 8 plus 0 (no individuals).

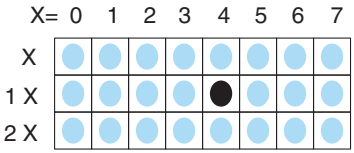


In the figure below, we have two groups of eight circles. Counting in octal we have "20."items, meaning two groups of eight, plus zero individuals Don't say "twenty," say "two–zero octal". This makes a clear distinction between number systems.



After *counting* PLC resources, it's time to access PLC resources (there's a difference). The CPU instruction set accesses resources of the PLC using octal addresses. Octal addresses are the same as octal quantities, except they start counting at zero. The number zero is significant to a computer, so we don't skip it.

Our circles are in an array of square containers to the right. To access a resource, our PLC instruction will address its location using the octal references shown. If these were counters, "CT14" would access the black circle location.

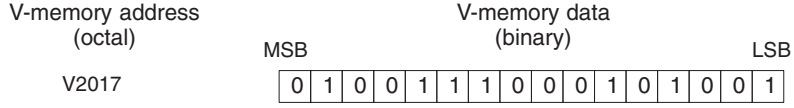


V–Memory

Variable memory (called "V-memory") stores data for the ladder program and for configuration settings. V-memory locations and V-memory addresses are the same thing, and are numbered in octal. For example, V2073 is a valid location, while V1983 is not valid ("9" and "8" are not valid octal digits).

Each V-memory location is one data word wide, meaning 16 bits. For configuration registers, our manuals will show each bit of a V-memory word. The least significant bit (LSB) will be on the right, and the most significant bit (MSB) on the left. We use the word "significant," referring to the relative binary weighting of the bits.

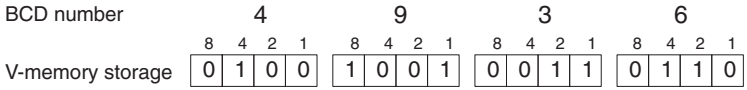
V-memory data is 16-bit binary, but we rarely program the data registers one bit at a time. We use



instructions or viewing tools that let us work with binary, decimal, octal, and hexadecimal numbers. All these are converted and stored as binary for us. A frequently-asked question is "How do I tell if a number is binary, octal, BCD, or hex"? The answer is that we usually cannot tell by looking at the data, but it does not really matter. What matters is: the source or mechanism which writes data into a V-memory location and the thing which later reads it must both use the same data type (i.e., octal, hex, binary, or whatever). The V-memory location is a storage box, that's all. It does not convert or move the data on its own.

Binary-Coded Decimal Numbers

Since humans naturally count in decimal, we prefer to enter and view PLC data in decimal as well (via operator interfaces). However, computers are more efficient in using pure binary numbers. A compromise solution between the two is Binary-Coded Decimal (BCD) representation. A BCD digit ranges from 0 to 9, and is stored as 4 binary bits (a nibble). This permits each V-memory location to store 4 BCD digits, with a range of decimal numbers from 0000 to 9999.



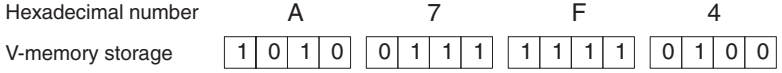
In a pure binary sense, a 16-bit word represents numbers from 0 to 65535. In storing BCD numbers, the range is reduced to 0 to 9999. Many math instructions use BCD data, and *Direct*SOFT and the Handheld Programmer allow us to enter and view data in BCD. Special RLL instructions convert from BCD to binary, or visa–versa.

Hexadecimal Numbers

Hexadecimal numbers are similar to BCD numbers, except they utilize all possible binary values in each 4-bit digit. They are base-16 numbers so we need 16 different digits. To extend our decimal digits 0 through 9, we use A through F as shown.

Decimal	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Hexadecimal	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F

A 4-digit hexadecimal number can represent all 65536 values in a V-memory word. The range is from 0000 to FFFF (hex). PLCs often need this full range for sensor data, etc. Hexadecimal is a convenient way for humans to view full binary data.

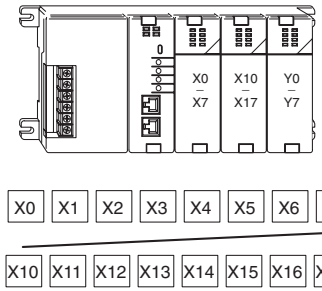


Memory Map

With any PLC system, you generally have many different types of information to process. This includes input device status, output device status, various timing elements, parts counts, etc. It is important to understand how the system represents and stores the various types of data. For example, you need to know how the system identifies input points, output points, data words, etc. The following paragraphs discuss the various memory types used in the DL205 CPUs. A memory map overview for the DL230, DL240, DL250–1 and DL260 CPUs follows the memory descriptions.

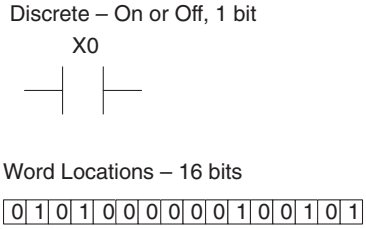
Octal Numbering System

All memory locations or areas are numbered in Octal (base 8). For example, the diagram shows how the octal numbering system works for the discrete input points. Notice the octal system does not contain any numbers with the digits 8 or 9.



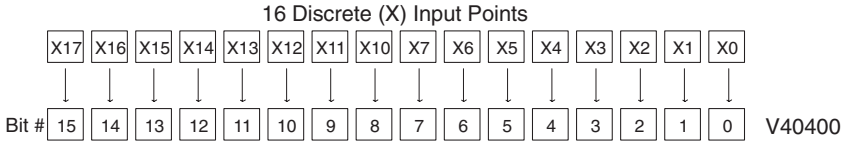
Discrete and Word Locations

As you examine the different memory types, you'll notice two types of memory in the DL205, discrete and word memory. Discrete memory is one bit that can be either a 1 or a 0. Word memory is referred to as V memory (variable) and is a 16-bit location normally used to manipulate data/numbers, store data/numbers, etc. Some information is automatically stored in V-memory. For example, the timer current values are stored in V-memory.



V–Memory Locations for Discrete Memory Areas

The discrete memory area is for inputs, outputs, control relays, special relays, stages, timer status bits and counter status bits. However, you can also access the bit data types as a V-memory word. Each V-memory location contains 16 consecutive discrete locations. For example, the following diagram shows how the X input points are mapped into V-memory locations.



These discrete memory areas and their corresponding V-memory ranges are listed in the memory area table for the DL230, DL240, DL250–1 and DL260 CPUs in this chapter.

Input Points (X Data Type)

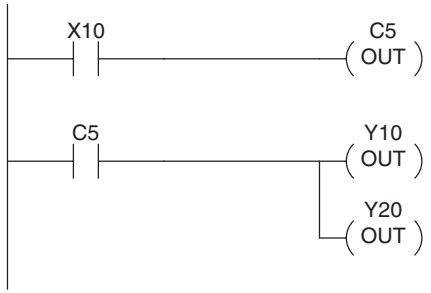
The discrete input points are noted by an X data type. Up to 512 discrete input points are available with the DL205 CPUs. In this example, the output point Y0 will be turned on when input X0 energizes.

Output Points (Y Data Type)

The discrete output points are noted by a Y data type. Up to 512 discrete output points are available with the DL205 CPUs. In this example, output point Y1 will turn on when input X1 energizes.

Control Relays (C Data Type)

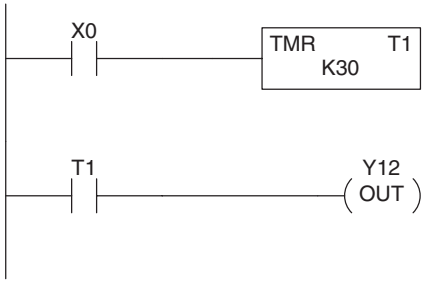
Control relays are discrete bits normally used to control the user program. The control relays do not represent a real world device; that is, they cannot be physically tied to switches, output coils, etc. Control relays are internal to the CPU and can be programmed as discrete inputs or discrete outputs. These locations are used in programming the discrete memory locations (C) or the corresponding word location which has 16 consecutive discrete locations. In this example, memory location C5 will energize when input X10 turns on. The second rung shows a simple example of how to use a control relay as an input.



Timers and Timer Status Bits (T Data Type)

The number of timers available depends on the model of CPU you are using. The tables at the end of this section provide the number of timers for the DL230, DL240, D2-250-1 and DL260. Regardless of the number of timers, you have access to timer status bits that reflect the relationship between the current value and the preset value of a specified timer. The timer status bit will be on when the current value is equal to or greater than the preset value of a corresponding timer.

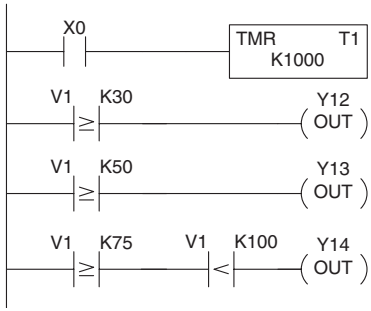
When input X0 turns on, timer T1 will start. When the timer reaches the preset of 3 seconds (K of 30), timer status contact T1 turns on. When T1 turns on, output Y12 turns on.



Timer Current Values (V Data Type)

Some information is automatically stored in V-memory, such as the current values associated with timers. For example, V0 holds the current value for Timer 0, V1 holds the current value for Timer 1, etc. These are 4-digit BCD values.

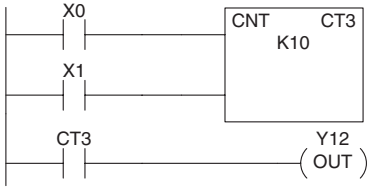
The primary reason for this is programming flexibility. The example shows how you can use relational contacts to monitor several time intervals from a single timer.



Counters and Counter Status Bits (CT Data Type)

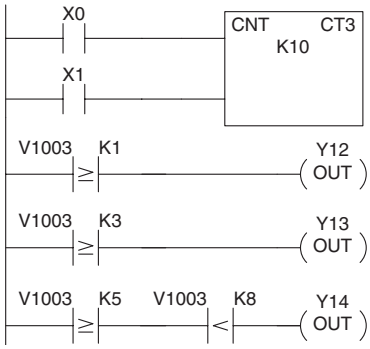
You have access to counter status bits that reflect the relationship between the current value and the preset value of a specified counter. The counter status bit will be on when the current value is equal to or greater than the preset value of a corresponding counter.

Each time contact X0 transitions from off to on, the counter increments by one (If X1 comes on, the counter is reset to zero). When the counter reaches the preset of 10 counts (K of 10), counter status contact CT3 turns on. When CT3 turns on, output Y12 turns on.



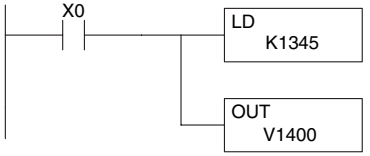
Counter Current Values (V Data Type)

Just like the timers, the counter current values are also automatically stored in V-memory. For example, V1000 holds the current value for Counter CT0, V1001 holds the current value for Counter CT1, etc. These are 4-digit BCD values. The primary reason for this is programming flexibility. The example shows how you can use relational contacts to monitor the counter values.

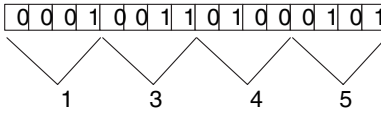


Word Memory (V Data Type)

Word memory is referred to as V-memory (variable) and is a 16-bit location normally used to manipulate data/numbers, store data/numbers, etc. Some information is automatically stored in V-memory. For example, the timer current values are stored in V-memory. The example shows how a four-digit BCD constant is loaded into the accumulator and then stored in a V-memory location.



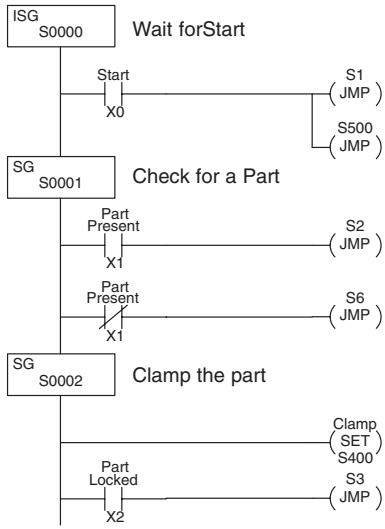
Word Locations – 16 bits



Stages (S Data type)

Stages are used in RLL*PLUS* programs to create a structured program, similar to a flowchart. Each program stage denotes a program segment. When the program segment, or stage, is active, the logic within that segment is executed. If the stage is off, or inactive, the logic is not executed and the CPU skips to the next active stage. (See Chapter 7 for a more detailed description of RLL*PLUS* programming.)

Each stage also has a discrete status bit that can be used as an input to indicate whether the stage is active or inactive. If the stage is active, then the status bit is on. If the stage is inactive, then the status bit is off. This status bit can also be turned on or off by other instructions, such as the SET or RESET instructions. This allows you to easily control stages throughout the program.



Special Relays (SP Data Type)

Special relays are discrete memory locations with pre-defined functionality. There are many different types of special relays. For example, some aid in program development, others provide system operating status information, etc. Appendix D provides a complete listing of the special relays.

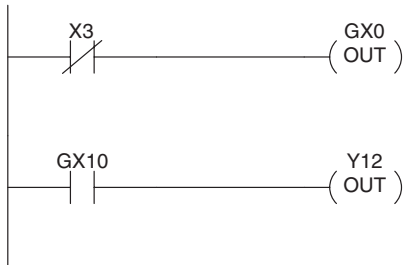
In this example, control relay C10 will energize for 50ms and de–energize for 50 ms because SP5 is a pre–defined relay that will be on for 50ms and off for 50ms.

SP4: 1 second clock
SP5: 100 ms clock
SP6: 50 ms clock

Remote I/O Points (GX Data Type)

Remote I/O points are represented by global relays. They are generally used only to control remote I/O, but they can be used as normal control relays when remote I/O is not used in the system.

In this example, memory location GX0 represents an output point and memory location GX10 represents an input point.



DL230 System V-memory

System V-memory	Description of Contents	Default Values/Ranges
V2320–V2377	The default location for multiple preset values for the UP counter.	N/A
V7620–V7627	Locations for DV–1000 operator interface parameters	
V7620	Sets the V-memory location that contains the value.	V0–V2377
V7621	Sets the V-memory location that contains the message.	V0–V2377
V7622	Sets the total number (1 - 16) of V-memory locations to be displayed.	1–16
V7623	Sets the V-memory location that contains the numbers to be displayed.	V0–V2377
V7624	Sets the V-memory location that contains the character code to be displayed.	V0–V2377
V7625	Sets the bit control pointer.	V-memory location for X,Y, or C points used.
V7626	Power Up mode change preset value password.	0,1,2,3,12 Default = 0000
V7627	Reserved for future use.	
V7630	Starting location for the multi–step presets for channel 1. The default value is 2320, which indicates the first value should be obtained from V2320. Since 24 presets are available, the default range is V2320 – V2377. You can change the starting point if necessary.	Default: V2320 Range: V0–V2320
V7631–V7632	Not used	N/A
V7633	Sets the desired mode for the high speed counter, interrupt, pulse catch, pulse train, and input filter (see the D2-CTRINT Manual, D2-CTRIF-M for more information). Location is also used for setting the with/without battery option, enable/disable CPU mode change, and power-up in Run Mode option.	Default: 0000 Lower Byte Range: Range: 0–None 10–Up 40–Interrupt 50–Pulse Catch 60–Filtered discrete In. Upper Byte Range: Bits 8–11, 14,15: Unused Bit 12: With Batt. installed: 0 = disable BATT LED 1 = enable BATT LED Bit 13: Power-up in Run
V7634	Contains set-up information for high-speed counter, interrupt, pulse catch, pulse train output, and input filter for X0 (when D2–CTRINT is installed).	Default: 0000
V7635	Contains set up-information for high-speed counter, interrupt, pulse catch, pulse train output, and input filter for X1 (when D2–CTRINT is installed).	Default: 0000
V7636	Contains set-up information for high-speed counter, interrupt, pulse catch, pulse train output, and input filter for X2 (when D2–CTRINT is installed).	Default: 0000
V7637	Contains set-up information for high-speed counter, interrupt, pulse catch, pulse train output, and input filter for X3 (when D2–CTRINT is installed).	Default: 0000
V7640–V7642	Additional setup parameters for the DV-1000	
V7640	Timer preset value pointer	V2000–V2377
V7641	Counter preset value pointer	V2000–V2377
V7642	Timer preset block size (high byte) / Counter preset block size (low byte)	1–99
V7643–V7647	Not used	N/A
V7751	Fault Message Error Code — stores the 4-digit code used with the FAULT instruction when the instruction is executed.	N/A

System V-memory	Description of Contents	Default Values/Ranges
V7752	I/O Configuration Error — stores the module ID code for the module that does not match the current configuration.	N/A
V7753	I/O Configuration Error — stores the correct module ID code.	
V7754	I/O Configuration Error — identifies the base and slot number.	
V7755	Error code — stores the fatal error code.	N/A
V7756	Error code — stores the major error code.	N/A
V7757	Error code — stores the minor error code.	
V7760–V7764	Module Error — stores the slot number and error code where an I/O error occurs.	
V7765	Scan — stores the total number of scan cycles that have occurred since the last Program Mode to Run Mode transition.	
V7666–V7774	Not used	N/A
V7775	Scan — stores the current scan time (milliseconds).	N/A
V7776	Scan — stores the minimum scan time that has occurred since the last Program Mode to Run Mode transition (milliseconds).	N/A
V7777	Scan — stores the maximum scan time that has occurred since the last Program Mode to Run Mode transition (milliseconds).	N/A

DL240 System V-memory

System V-memory	Description of Contents	Default Values/ Ranges
V3630–V3707	The default location for multiple preset values for UP/DWN and UP counter 1 or pulse output function.	N/A
V3710–V3767	The default location for multiple preset values for UP/DWN and UP counter 2.	N/A
V3770–V3773	Not used	N/A
V3774–V3777	Default locations for analog potentiometer data (channels 1–4, respectively).	Range: 0 – 9999
V7620–V7627 V7620 V7621 V7622 V7623 V7624 V7625 V7626 V7627	Locations for DV–1000 operator interface parameters Sets the V-memory location that contains the value. Sets the V-memory location that contains the message. Sets the total number (1 – 16) of V-memory locations to be displayed. Sets the V-memory location that contains the numbers to be displayed. Sets the V-memory location that contains the character code to be displayed. Sets the bit control pointer Power Up Mode Change Preset Value Password.	 V0 – V3760 V0 – V3760 1 – 16 V0 – V3760 V0 – V3760 V-memory location for X, Y, or C points used. 0,1,2,3,12 Default=0000
V7630	Starting location for the multi–step presets for channel 1. Since there are 24 presets available, the default range is V3630 – V3707. You can change the starting point if necessary.	Default: V3630 Range: V0 – V3710
V7631	Starting location for the multi–step presets for channel 2. Since there are 24 presets available, the default range is V3710– V3767. You can change the starting point if necessary.	Default: V3710 Range: V0 – V3710
V7632	Contains the baud rate setting for Port 2. You can use AUX 56 (from the Handheld Programmer) or, use ***Direct***SOFT to set the port parameters if 9600 baud is unacceptable. Also allows you to set a delay time between the assertion of the RTS signal and the transmission of data. This is useful for radio modems that require a key-up delay before data is transmitted. e.g., a value of 0302 sets 10ms Turnaround Delay (TAD) and 9600 baud.	Default: 2 – 9600 baud Lower Byte = Baud Rate Lower Byte Range: 00 = 300 01 = 1200 02 = 9600 03 = 19.2K Upper Byte = Time Delay Upper Byte Range: 01 = 2ms 02 = 5ms 03 = 10ms 04 = 20ms 05 = 50ms 06 = 100ms 07 = 500ms

System V-memory	Description of Contents	Default Values/ Ranges
V7633	Sets the desired mode for the high speed counter, interrupt, pulse catch, pulse train, and input filter (see the D2-CTRINT manual, D2-CTRIF-M, for more information). Location is also used for setting the with/without battery option, enable/disable CPU mode change.	Default: 0000 Lower Byte Range: 0 – None 10 – Up 20 – Up/Dwn. 30 – Pulse Out 40 – Interrupt 50 – Pulse Catch 60 – Filtered Dis. Upper Byte Range: Bits 8 – 11, 15 Unused Bit 12: With Batt. installed: 0 = disable BATT LED 1 = enable BATT LED Bit 13: Power-up in Run Bit 14: Mode chg. enable (K-sequence only)
V7634	Contains set-up information for high-speed counter, interrupt, pulse catch, pulse train output, and input filter for X0 (when D2–CTRINT is installed).	Default: 0000
V7635	Contains set-up information for high-speed counter, interrupt, pulse catch, pulse train output, and input filter for X1 (when D2–CTRINT is installed).	Default: 0000
V7636	Contains set-up information for high-speed counter, interrupt, pulse catch, pulse train output, and input filter for X2 (when D2–CTRINT is installed).	Default: 0000
V7637	Contains set-up information for high-speed counter, interrupt, pulse catch, pulse train output, and input filter for X3 (when D2–CTRINT is installed).	Default: 0000
V7640–V7641	Location for setting the lower and upper limits for the CH1 analog pot.	Default: 0000 Range: 0 – 9999
V7642–V7643	Location for setting the lower and upper limits for the CH2 analog pot.	Default: 0000 Range: 0 – 9999
V7644–V7645	Location for setting the lower and upper limits for the CH3 analog pot.	Default: 0000 Range: 0 – 9999
V7646–V7647	Location for setting the lower and upper limits for the CH4 analog pot.	Default: 0000 Range: 0 – 9999
V7650–V7737	Locations reserved for set-up information used with future options (remote I/O and data communications).	
V7720–V7722	Locations for DV–1000 operator interface parameters.	
V7720	Titled Timer preset value pointer .	V2000–V2377
V7721	Titled Counter preset value pointer.	V2000–V2377
V7722	HiByte-Titled Timer preset block size, LoByte-Titled Counter preset block size.	1–99
V7746	Location contains the battery voltage, accurate to 0.1V. For example, a value of 32 indicates 3.2 volts.	
V7747	Location contains a 10ms counter. This location increments once every 10ms.	
V7751	Fault Message Error Code — stores the 4-digit code used with the FAULT instruction when the instruction is executed. If you've used ASCII messages (DL240 only), then the data label (DLBL) reference number for that message is stored here.	
V7752	I/O configuration Error — stores the module ID code for the module that does not match the current configuration.	

System V-memory	Description of Contents
V7753	I/O Configuration Error — stores the correct module ID code.
V7754	I/O Configuration Error — identifies the base and slot number.
V7755	Error code — stores the fatal error code.
V7756	Error code — stores the major error code.
V7757	Error code — stores the minor error code.
V7760–V7764	Module Error — stores the slot number and error code where an I/O error occurs.
V7765	Scan—stores the number of scan cycles that have occurred since the last Program to Run Mode transition.
V7766	Contains the number of seconds on the clock. (00 to 59).
V7767	Contains the number of minutes on the clock. (00 to 59).
V7770	Contains the number of hours on the clock. (00 to 23).
V7771	Contains the day of the week. (Mon, Tue, etc.).
V7772	Contains the day of the month (1st, 2nd, etc.).
V7773	Contains the month. (01 to 12)
V7774	Contains the year. (00 to 99)
V7775	Scan — stores the current scan time (milliseconds).
V7776	Scan — stores the minimum scan time that has occurred since the last Program Mode to Run Mode transition (milliseconds).
V7777	Scan — stores the maximum scan time that has occurred since the last Program Mode to Run Mode transition (milliseconds).

DL250–1 System V-memory (DL250 also)

System V-memory	Description of Contents	Default Values/ Ranges
V3630–V3707	The default location for multiple preset values for UP/DWN and UP counter 1 or pulse output function	N/A
V3710–V3767	The default location for multiple preset values for UP/DWN and UP counter 2.	N/A
V3770–V3777	Not used	N/A
V7620–V7627	Locations for DV–1000 operator interface parameters	
V7620	Sets the V-memory location that contains the value	V0 – V3760
V7621	Sets the V-memory location that contains the message	V0 – V3760
V7622	Sets the total number (1 – 32) of V-memory locations to be displayed	1 – 32
V7623	Sets the V-memory location that contains the numbers to be displayed	V0 – V3760
V7624	Sets the V-memory location that contains the character code to be displayed	V0 – V3760
V7625	Sets the bit control pointer	V-memory for X, Y, or C
V7626	Sets the power up mode	0,1,2,3,12
V7627	Change Preset Value password	Default=0000
V7630	Starting location for the multi–step presets for channel 1. Since there are 24 presets available, the default range is V3630 – V3707. You can change the starting point if necessary.	Default: V3630 Range: V0 – V3710
V7631	Starting location for the multi–step presets for channel 2. Since there are 24 presets available, the default range is V3710– V3767. You can change the starting point if necessary.	Default: V3710 Range: V0 – V3710
V7632	Reserved	
V7633	Sets the desired mode for the high-speed counter, interrupt, pulse catch, pulse train, and input filter (see the D2-CTRINT manual, D2-CTRIF-M, for more information). Location is also used for setting the with/without battery option, enable/disable CPU mode change, and power-up in Run Mode option.	Default: 0060 Lower Byte Range: Range: 0 – None 10 – Up 20 – Up/Dwn. 30 – Pulse Out 40 – Interrupt 50 – Pulse Catch 60 – Filtered Dis. Upper Byte Range: Bits 8 – 11, 14–15 Unused Bit 12: With Batt. installed: 0 = disable BATT LED 1 = enable BATT LED Bit 13: Power-up in Run
V7634	Contains set-up information for high-speed counter, interrupt, pulse catch,pulse train output, and input filter for X0 (when D2–CTRINT is installed).	Default: 1006
V7635	Contains set-up information for high-speed counter, interrupt, pulse catch, pulse train output, and input filter for X1 (when D2–CTRINT is installed).	Default: 1006
V7636	Contains set-up information for high-speed counter, interrupt, pulse catch, pulse train output, and input filter for X2 (when D2–CTRINT is installed).	Default: 1006

System V-memory	Description of Contents	Default Values/Ranges
V7637	Contains set-up information for high-speed counter, interrupt, pulse catch, pulse train output, and input filter for X3 (when D2–CTRINT is installed).	Default: 1006
V7640	Loop Table Beginning address.	V1400–V7340 V10000–V17740
V7641	Number of Loops Enabled	1–4
V7642	Error Code – V–memory Error Location for Loop Table.	
V7643–V7647	Reserved.	
V7650	Port 2 End–code setting Setting (A55A), Non–procedure communications start.	
V7651	Port 2 Data format – Non–procedure communications format setting.	
V7652	Port 2 Format Type setting – Non–procedure communications type code setting.	
V7653	Port 2 Terminate–code setting – Non–procedure communications Termination code setting.	
V7654	Port 2 Store v–mem address – Non–procedure communication data store V–Memory address	
V7655	Port 2 Setup area –0–7 Comm protocol (flag 0) 8–15 Comm time out/response delay time (flag 1).	
V7656	Port 2 Setup area – 0–15 Communication (flag 2, flag 3).	
V7657	Port 2: Setup completion code.	
V7660–V7717	Set–up Information – Locations reserved for set-up information used with future options.	
V7720–V7722	Locations for DV–1000 operator interface parameters.	
V7720	Titled Timer preset value pointer.	
V7721	Title Counter preset value pointer.	
V7722	HiByte-Titled Timer preset block size, LoByte-Titled Counter preset block size.	
V7740	Port 2 Communication Auto Reset Timer setup.	
V7741	Output Hold or reset setting: Expansion bases 1 and 2 (DL250–1).	
V7747	Location contains a 10ms counter. This location increments once every 10ms.	
V7750	Reserved.	
V7751	Fault Message Error Code — stores the 4-digit code used with the FAULT instruction when the instruction is executed. If you've used ASCII messages (DL240 only), then the data label (DLBL) reference number for that message is stored here.	
V7752	I/O configuration Error — stores the module ID code for the module that does not match the current configuration.	
V7753	I/O Configuration Error — stores the correct module ID code.	
V7754	I/O Configuration Error — identifies the base and slot number.	
V7755	Error code — stores the fatal error code.	
V7756	Error code — stores the major error code.	
V7757	Error code — stores the minor error code.	
V7760–V7764	Module Error — stores the slot number and error code where an I/O error occurs.	
V7765	Scan — stores the total number of scan cycles that have occurred since the last Program Mode to Run Mode transition.	

System V-memory	Description of Contents
V7766	Contains the number of seconds on the clock. (00 to 59)
V7767	Contains the number of minutes on the clock. (00 to 59)
V7770	Contains the number of hours on the clock. (00 to 23)
V7771	Contains the day of the week. (Mon, Tue, etc.)
V7772	Contains the day of the month (1st, 2nd, etc.)
V7773	Contains the month. (01 to 12)
V7774	Contains the year. (00 to 99)
V7775	Scan — stores the current scan time (milliseconds)
V7776	Scan — stores the minimum scan time that has occurred since the last Program Mode to Run Mode transition (milliseconds)
V7777	Scan — stores the maximum scan time that has occurred since the last Program Mode to Run Mode transition (milliseconds)
V36000–36057	Analog pointer method for expansion base 1 (DL250–1)
V36100–36157	Analog pointer method for expansion base 2 (DL250–1)
V36400–36427	Analog pointer method for local base
V37700–37737	Port 2: Setup register for Koyo Remote I/O

System CRs	Description of Contents
C740	Completion of setups – ladder logic must turn this relay on when it has finished writing to the Remote I/O setup table.
C741	Erase received data – turning on this flag will erase the received data during a communication error.
C743	Re-start – Turning on this relay will resume after a communications hang-up on an error.
C750 to C757	Setup Error – The corresponding relay will be ON if the setup table contains an error. (C750 = master, C751 = slave 1 C757 = slave 7)
C760 to C767	Communications Ready – The corresponding relay will be ON if the set-up table data is valid. (C760 = master, C761 = slave 1 C767 = slave 7)

DL260 System V-memory

System V-memory	Description of Contents	Default Values/Ranges
V3630–V3707	The default location for multiple preset values for UP/DWN and UP counter 1 or pulse output function	N/A
V3710–V3767	The default location for multiple preset values for UP/DWN and UP counter 2	N/A
V3770–V3777	Not used	N/A
V7620–V7627 V7620 V7621 V7622 V7623 V7624 V7625 V7626 V7627	Locations for DV–1000 operator interface parameters Sets the V-memory location that contains the value Sets the V-memory location that contains the message Sets the total number (1 – 32) of V-memory locations to be displayed Sets the V-memory location that contains the numbers to be displayed Sets the V-memory location that contains the character code to be displayed Sets the bit control pointer Sets the power up mode Change Preset Value password	 V0 – V3760 V0 – V3760 1 – 32 V0 – V3760 V0 – V3760 V-memory for X, Y, or C 0,1,2,3,12 Default=0000
V7630	Starting location for the multi–step presets for channel 1. Since there are 24 presets available, the default range is V3630 – V3707. You can change the starting point if necessary.	Default: V3630 Range: V0 – V3710
V7631	Starting location for the multi–step presets for channel 2. Since there are 24 presets available, the default range is V3710– V3767. You can change the starting point if necessary.	Default: V3710 Range: V0 – V3710
V7632	Reserved	
V7633	Sets the desired mode for the high-speed counter, interrupt, pulse catch, pulse train, and input filter (see the D2-CTRINT manual, D2-CTRIF-M, for more information). Location is also used for setting the with/without battery option, enable/disable CPU mode change, and power-up in Run Mode option.	Default: 0060 Lower Byte Range: Range: 0 – None 10 – Up 20 – Up/Dwn 30 – Pulse Ou 40 – Interrupt 50 – Pulse Catch 60 – Fltered Dis. Upper Byte Range Bits 8 – 11, 14–15 Unused Bit 12: With Batt. installed: 0 = disable BATT LED 1 = enable BATT LED Bit 13: Power-up in Run
V7634	Contains set-up information for high-speed counter, interrupt, pulse catch, pulse train output, and input filter for X0 (when D2–CTRINT is installed)	Default: 1006
V7635	Contains set-up information for high-speed counter, interrupt, pulse catch, pulse train output, and input filter for X1 (when D2–CTRINT is installed)	Default: 1006
V7636	Contains set-up information for high-speed counter, interrupt, pulse catch, pulse train output, and input filter for X2 (when D2–CTRINT is installed)	Default: 1006

System V-memory	Description of Contents	Default Values/ Ranges
V7637	Contains set up information for high speed counter, interrupt, pulse catch, pulse train output, and input filter for X3 (when D2–CTRINT is installed).	Default: 1006
V7640	PID Loop Table Beginning address.	V400–640 V1400–V7340 V10000–V35740
V7641	Number of Loops Enabled.	1–16
V7642	Error Code – V–memory Error Location for Loop Table.	
V7643 - V7647	Reserved.	
V7650	Port 2 End–code Setting (A55A), Non-procedure communications start.	
V7651	Port 2 Data format - Non-procedure communications format setting.	
V7652	Port 2 Format Type setting – Non–procedure communications type code setting.	
V7653	Port 2 Terminate–code setting – Non–procedure communications Termination code setting	
V7654	Port 2 Store v–mem address – Non–procedure communication data store V–Memory address.	
V7655	Port 2 Setup area –0–7 Comm protocol (flag 0) 8–15 Comm time out/response delay time (flag 1)	
V7656	Port 2 Setup area – 0–15 Communication (flag 2, flag 3)	
V7657	Port 2: Setup completion code.	
V7660–V7717	Set–up Information – Locations reserved for set up information used with future options.	
V7720–V7722 V7720 V7721 V7722	Locations for DV-1000 operator interface parameters. Titled Timer preset value pointer. Title Counter preset value pointer. HiByte-Titled Timer preset block size, LoByte-Titled Counter preset block size.	
V7740	Port 2 Communication Auto Reset Timer setup.	
V7741	Output Hold or reset setting: Expansion bases 1 and 2.	
V7742	Output Hold or reset setting: Expansion bases 3 and 4.	
V7747	Location contains a 10ms counter. This location increments once every 10ms.	
V7750	Reserved.	
V7751	Fault Message Error Code — stores the 4-digit code used with the FAULT instruction when the instruction is executed. If you've used ASCII messages (DL240 only), then the data label (DLBL) reference number for that message is stored here.	
V7752	I/O configuration Error — stores the module ID code for the module that does not match the current configuration.	
V7753	I/O Configuration Error — stores the correct module ID code.	
V7754	I/O Configuration Error — identifies the base and slot number.	
V7755	Error code — stores the fatal error code.	
V7756	Error code — stores the major error code.	
V7757	Error code — stores the minor error code.	
V7763–V7764	Module Error — stores the slot number and error code where an I/O error occurs.	
V7765	Scan — stores the total number of scan cycles that have occurred since the last Program Mode to Run Mode transition.	

System V-memory	Description of Contents
V7766	Contains the number of seconds on the clock. (00 to 59).
V7767	Contains the number of minutes on the clock. (00 to 59).
V7770	Contains the number of hours on the clock. (00 to 23).
V7771	Contains the day of the week. (Mon, Tue, etc.).
V7772	Contains the day of the month (1st, 2nd, etc.).
V7773	Contains the month. (01 to 12)
V7774	Contains the year. (00 to 99)
V7775	Scan — stores the current scan time (milliseconds).
V7776	Scan — stores the minimum scan time that has occurred since the last Program Mode to Run Mode transition (milliseconds).
V7777	Scan — stores the maximum scan time that has occurred since the last Program Mode to Run Mode transition (milliseconds).
V36000–36057	Analog pointer method for expansion base 1
V36100–36157	Analog pointer method for expansion base 2
V36200–36257	Analog pointer method for expansion base 3
V36300–36357	Analog pointer method for expansion base 4
V36400–36427	Analog pointer method for local base
V37700–37737	Port 2: Set-up register for Koyo Remote I/O

The following system control relays are used for Koyo Remote I/O setup on Communications Port 2.

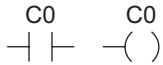
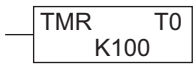
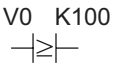
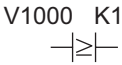
System CRs	Description of Contents
C740	Completion of setups – ladder logic must turn this relay on when it has finished writing to the Remote I/O setup table.
C741	Erase received data – turning on this flag will erase the received data during a communication error.
C743	Re-start – Turning on this relay will resume after a communications hang-up on an error.
C750 to C757	Setup Error – The corresponding relay will be ON if the set-up table contains an error. (C750 = master, C751 = slave 1... C757= slave 7
C760 to C767	Communications Ready – The corresponding relay will be ON if the set-up table data is valid. (C760 = master, C761 = slave 1...C767 = slave 7

DL205 Aliases

An alias is an alternate way of referring to certain memory types, such as timer/counter current values, V-memory locations for I/O points, etc., which simplifies understanding the memory address. The use of the alias is optional, but some users may find the alias to be helpful when developing a program. The table below shows how the aliases can be used.

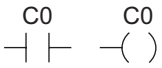
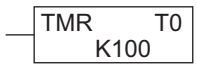
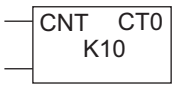
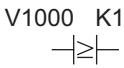
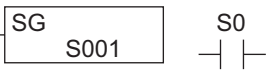
DL205 Aliases		
Address Start	**Alias Start**	**Example**
V0	TA0	V0 is the timer accumulator value for timer 0, therefore, its alias is TA0. TA1 is the alias for V1, etc.
V1000	CTA0	V1000 is the counter accumulator value for counter 0, therefore, its alias is CTA0. CTA1 is the alias for V1001, etc.
V40000	VGX	V40000 is the word memory reference for discrete bits GX0 through GX17, therefore, its alias is VGX0. V40001 is the word memory reference for discrete bits GX20 through GX37, therefore, its alias is VGX20.
V40200	VGY	V40200 is the word memory reference for discrete bits GY0 through GY17, therefore, its alias is VGY0. V40201 is the word memory reference for discrete bits GY20 through GY37, therefore, its alias is VGY20.
V40400	VX0	V40400 is the word memory reference for discrete bits X0 through X17, therefore, its alias is VX0. V40401 is the word memory reference for discrete bits X20 through X37, therefore, its alias is VX20.
V40500	VY0	V40500 is the word memory reference for discrete bits Y0 through Y17, therefore, its alias is VY0. V40501 is the word memory reference for discrete bits Y20 through Y37, therefore, its alias is VY20.
V40600	VC0	V40600 is the word memory reference for discrete bits C0 through C17, therefore, its alias is VC0. V40601 is the word memory reference for discrete bits C20 through C37, therefore, its alias is VC20.
V41000	VS0	V41000 is the word memory reference for discrete bits S0 through S17, therefore, its alias is VS0. V41001 is the word memory reference for discrete bits S20 through S37, therefore, its alias is VS20.
V41100	VT0	V41100 is the word memory reference for discrete bits T0 through T17, therefore, its alias is VT0. V41101 is the word memory reference for discrete bits T20 through T37, therefore, its alias is VT20.
V41140	VCT0	V41140 is the word memory reference for discrete bits CT0 through CT17, therefore, its alias is VCT0. V41141 is the word memory reference for discrete bits CT20 through CT37, therefore, its alias is VCT20.
V41200	VSP0	V41200 is the word memory reference for discrete bits SP0 through SP17, therefore, its alias is VSP0. V41201 is the word memory reference for discrete bits SP20 through SP37, therefore, its alias is VSP20.

DL230 Memory Map

Memory Type	Discrete Memory Reference (octal)	Word Memory Reference (octal)	Qty. Decimal	Symbol
Input Points	X0 – X177	V40400 – V40407	128[1]	
Output Points	Y0 – Y177	V40500 – V40507	128[1]	
Control Relays	C0 – C377	V40600 – V40617	256	
Special Relays	SP0 – SP117 SP540 – SP577	V41200 – V41204 V41226 – V41227	112	
Timers	T0 – T77		64	
Timer Current Values	None	V0 – V77	64	
Timer Status Bits	T0 – T77	V41100 – V41103	64	
Counters	CT0 – CT77		64	
Counter Current Values	None	V1000 – V1077	64	
Counter Status Bits	CT0 – CT77	V41140 – V41143	64	
Data Words	None	V2000 – V2377	256	None specific, used with many instructions
Data Words Non–volatile	None	V4000 – V4177	128	None specific, used with many instructions
Stages	S0 – S377	V41000 – V41017	256	
System parameters	None	V7620 – V7647 V7750–V7777	48	None specific, used for various purposes

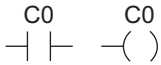
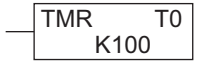
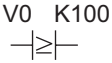
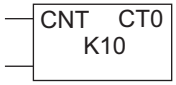
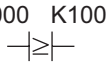
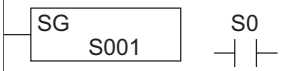
NOTE 1: *The DL230 systems are limited to 256 discrete I/O points (total) with the present system hardware available. These can be mixed between inputs and output points as necessary.*

DL240 Memory Map

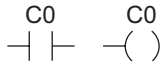
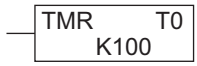
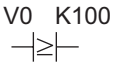
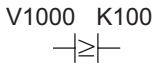
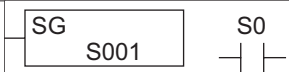
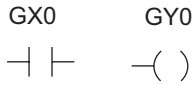
Memory Type	Discrete Memory Reference (octal)	Word Memory Reference(octal)	Qty. Decimal	Symbol
Input Points	X0 – X477	V40400 – V40423	320[1]	
Output Points	Y0 – Y477	V40500 – V40523	320[1]	
Control Relays	C0 – C377	V40600 – V40617	256	
Special Relays	SP0 – SP137 SP540 – SP617	V41200 – V41205 V41226 – V41230	144	
Timers	T0 – T177		128	
Timer Current Values	None	V0 – V177	128	
Timer Status Bits	T0 – T177	V41100 – V41107	128	
Counters	CT0 – CT177		128	
Counter Current Values	None	V1000 – V1177	128	
Counter Status Bits	CT0 – CT177	V41140 – V41147	128	
Data Words	None	V2000 – V3777	1024	None specific, used with many instructions
Data Words Non–volatile	None	V4000 – V4377	256	None specific, used with many instructions
Stages	S0 – S777	V41000 – V41037	512	
System parameters	None	V7620 – V7737 V7746–V7777	106	None specific, used for various purposes

NOTE 1: *The DL240 systems are limited to 256 discrete I/O points (total) with the present system hardware available. These can be mixed between inputs and output points as necessary.*

DL250–1 Memory Map (DL250 also)

Memory Type	Discrete Memory Reference (octal)	Word Memory Reference (octal)	Qty. Decimal	Symbol
Input Points	X0 – X777	V40400 – V40437	512	
Output Points	Y0 – Y777	V40500 – V40537	512	
Control Relays	C0 – C1777	V40600 – V40677	1024	
Special Relays	SP0 – SP777	V41200 – V41237	512	
Timers	T0 – T377		256	
Timer Current Values	None	V0 – V377	256	
Timer Status Bits	T0 – T377	V41100 – V41117	256	
Counters	CT0 – CT177		128	
Counter Current Values	None	V1000 – V1177	128	
Counter Status Bits	CT0 – CT177	V41140 – V41147	128	
Data Words	None	V1400 – V7377 V10000–V17777	7168	None specific, used with many instructions
Stages	S0 – S1777	V41000 – V41077	1024	
System parameters	None	V7400–V7777 V36000–V37777	768	None specific, used for various purposes

DL260 Memory Map

Memory Type	Discrete Memory Reference (octal)	Word Memory Reference (octal)	Qty. Decimal	Symbol
Input Points	X0 – X1777	V40400 – V40477	1024	
Output Points	Y0 – Y1777	V40500 – V40577	1024	
Control Relays	C0 – C3777	V40600 – V40777	2048	
Special Relays	SP0 – SP777	V41200 – V41237	512	
Timers	T0 – T377		256	
Timer Current Values	None	V0 – V377	256	
Timer Status Bits	T0 – T377	V41100 – V41117	256	
Counters	CT0 – CT377		256	
Counter Current Values	None	V1000 – V1377	256	
Counter Status Bits	CT0 – CT377	V41140 – V41157	256	
Data Words	None	V400 – V777 V1400 – V7377 V10000–V35777	14.6K	None specific, used with many instructions
Stages	S0 – S1777	V41000 – V41077	1024	
Remote Input and Output Points	GX0 – GX3777 GY0 – GY3777	V40000 – V40177 V40200–V40377	2048 2048	
System parameters	None	V7400–V7777 V36000–V37777	1.2K	None specific, used for various purposes

X Input/Y Output Bit Map

This table provides a listing of the individual Input points associated with each V-memory address bit for the DL230, DL240, and DL250–1 and DL260 CPUs. The DL250–1 ranges apply to the DL250.

MSB	DL230/DL240/DL250-1/DL260 Input (X) and Output (Y) Points															LSB	X Input	Y Output
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Address
017	016	015	014	013	012	011	010	007	006	005	004	003	002	001	000	V40400	V40500
037	036	035	034	033	032	031	030	027	026	025	024	023	022	021	020	V40401	V40501
057	056	055	054	053	052	051	050	047	046	045	044	043	042	041	040	V40402	V40502
077	076	075	074	073	072	071	070	067	066	065	064	063	062	061	060	V40403	V40503
117	116	115	114	113	112	111	110	107	106	105	104	103	102	101	100	V40404	V40504
137	136	135	134	133	132	131	130	127	126	125	124	123	122	121	120	V40405	V40505
157	156	155	154	153	152	151	150	147	146	145	144	143	142	141	140	V40406	V40506
177	176	175	174	173	172	171	170	167	166	165	164	163	162	161	160	V40407	V40507

MSB	DL240/DL250-1/DL260 Input (X) and Output (Y) Points															LSB		
217	216	215	214	213	212	211	210	207	206	205	204	203	202	201	200	V40410	V40510
237	236	235	234	233	232	231	230	227	226	225	224	223	222	221	220	V40411	V40511
257	256	255	254	253	252	251	250	247	246	245	244	243	242	241	240	V40412	V40512
277	276	275	274	273	272	271	270	267	266	265	264	263	262	261	260	V40413	V40513
317	316	315	314	313	312	311	310	307	306	305	304	303	302	301	300	V40414	V40514
337	336	335	334	333	332	331	330	327	326	325	324	323	322	321	320	V40415	V40515
357	356	355	354	353	352	351	350	347	346	345	344	343	342	341	340	V40416	V40516
377	376	375	374	373	372	371	370	367	366	365	364	363	362	361	360	V40417	V40517
417	416	415	414	413	412	411	410	407	406	405	404	403	402	401	400	V40420	V40520
437	436	435	434	433	432	431	430	427	426	425	424	423	422	421	420	V40421	V40521
457	456	455	454	453	452	451	450	447	446	445	444	443	442	441	440	V40422	V40522
477	476	475	474	473	472	471	470	467	466	465	464	463	462	461	460	V40423	V40523

MSB	Additional DL250-1/DL260 Input (X) and Output (Y) Points															LSB		
517	516	515	514	513	512	511	510	507	506	505	504	503	502	501	500	V40424	V40524
537	536	535	534	533	532	531	530	527	526	525	524	523	522	521	520	V40425	V40525
557	556	555	554	553	552	551	550	547	546	545	544	543	542	541	540	V40426	V40526
577	576	575	574	573	572	571	570	567	566	565	564	563	562	561	560	V40427	V40527
617	616	615	614	613	612	611	610	607	606	605	604	603	602	601	600	V40430	V40530
637	636	635	634	633	632	631	630	627	626	625	624	623	622	621	620	V40431	V40531
657	656	655	654	653	652	651	650	647	646	645	644	643	642	641	640	V40432	V40532
677	676	675	674	673	672	671	670	667	666	665	664	663	662	661	660	V40433	V40533
717	716	715	714	713	712	711	710	707	706	705	704	703	702	701	700	V40434	V40534
737	736	735	734	733	732	731	730	727	726	725	724	723	722	721	720	V40435	V40535
757	756	755	754	753	752	751	750	747	746	745	744	743	742	741	740	V40436	V40536
777	776	775	774	773	772	771	770	767	766	765	764	763	762	761	760	V40437	V40537

MSB	Additional DL260 Input (X) and Output (Y) Points															LSB	X Input	Y Output
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Address
1017	1016	1015	1014	1013	1012	1011	1010	1007	1006	1005	1004	1003	1002	1001	1000	**V40440**	**V40540**
1037	1036	1035	1034	1033	1032	1031	1030	1027	1026	1025	1024	1023	1022	1021	1020	**V40441**	**V40541**
1057	1056	1055	1054	1053	1052	1051	1050	1047	1046	1045	1044	1043	1042	1041	1040	**V40442**	**V40542**
1077	1076	1075	1074	1073	1072	1071	1070	1067	1066	1065	1064	1063	1062	1061	1060	**V40443**	**V40543**
1117	1116	1115	1114	1113	1112	1111	1110	1107	1106	1105	1104	1103	1102	1101	1100	**V40444**	**V40544**
1137	1136	1135	1134	1133	1132	1131	1130	1127	1126	1125	1124	1123	1122	1121	1120	**V40445**	**V40545**
1157	1156	1155	1154	1153	1152	1151	1150	1147	1146	1145	1144	1143	1142	1141	1140	**V40446**	**V40546**
1177	1176	1175	1174	1173	1172	1171	1170	1167	1166	1165	1164	1163	1162	1161	1160	**V40447**	**V40547**
1217	1216	1215	1214	1213	1212	1211	1210	1207	1206	1205	1204	1203	1202	1201	1200	**V40450**	**V40550**
1237	1236	1235	1234	1233	1232	1231	1230	1227	1226	1225	1224	1223	1222	1221	1220	**V40451**	**V40551**
1257	1256	1255	1254	1253	1252	1251	1250	1247	1246	1245	1244	1243	1242	1241	1240	**V40452**	**V40552**
1277	1276	1275	1274	1273	1272	1271	1270	1267	1266	1265	1264	1263	1262	1261	1260	**V40453**	**V40553**
1317	1316	1315	1314	1313	1312	1311	1310	1307	1306	1305	1304	1303	1302	1301	1300	**V40454**	**V40554**
1337	1336	1335	1334	1333	1332	1331	1330	1327	1326	1325	1324	1323	1322	1321	1320	**V40455**	**V40555**
1357	1356	1355	1354	1353	1352	1351	1350	1347	1346	1345	1344	1343	1342	1341	1340	**V40456**	**V40556**
1377	1376	1375	1374	1373	1372	1371	1370	1367	1366	1365	1364	1363	1362	1361	1360	**V40457**	**V40557**
1417	1416	1415	1414	1413	1412	1411	1410	1407	1406	1405	1404	1403	1402	1401	1400	**V40460**	**V40560**
1437	1436	1435	1434	1433	1432	1431	1430	1427	1426	1425	1424	1423	1422	1421	1420	**V40461**	**V40561**
1457	1456	1455	1454	1453	1452	1451	1450	1447	1446	1445	1444	1443	1442	1441	1440	**V40462**	**V40562**
1477	1476	1475	1474	1473	1472	1471	1470	1467	1466	1465	1464	1463	1462	1461	1460	**V40463**	**V40563**
1517	1516	1515	1514	1513	1512	1511	1510	1507	1506	1505	1504	1503	1502	1501	1500	**V40464**	**V40564**
1537	1536	1535	1534	1533	1532	1531	1530	1527	1526	1525	1524	1523	1522	1521	1520	**V40465**	**V40565**
1557	1556	1555	1554	1553	1552	1551	1550	1547	1546	1545	1544	1543	1542	1541	1540	**V40466**	**V40566**
1577	1576	1575	1574	1573	1572	1571	1570	1567	1566	1565	1564	1563	1562	1561	1560	**V40467**	**V40567**
1617	1616	1615	1614	1613	1612	1611	1610	1607	1606	1605	1604	1603	1602	1601	1600	**V40470**	**V40570**
1637	1636	1635	1634	1633	1632	1631	1630	1627	1626	1625	1624	1623	1622	1621	1620	**V40471**	**V40571**
1657	1656	1655	1654	1653	1652	1651	1650	1647	1646	1645	1644	1643	1642	1641	1640	**V40472**	**V40572**
1677	1676	1675	1674	1673	1672	1671	1670	1667	1666	1665	1664	1663	1662	1661	1660	**V40473**	**V40573**
1717	1716	1715	1714	1713	1712	1711	1710	1707	1706	1705	1704	1703	1702	1701	1700	**V40474**	**V40574**
1737	1736	1735	1734	1733	1732	1731	1730	1727	1726	1725	1724	1723	1722	1721	1720	**V40475**	**V40575**
1757	1756	1755	1754	1753	1752	1751	1750	1747	1746	1745	1744	1743	1742	1741	1740	**V40476**	**V40576**
1777	1776	1775	1774	1773	1772	1771	1770	1767	1766	1765	1764	1763	1762	1761	1760	**V40477**	**V40577**

Control Relay Bit Map

This table provides a listing of the individual control relays associated with each V-memory address bit.

MSB	DL230/DL240/DL250-1/DL260 Control Relays (C)															LSB	Address
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
017	016	015	014	013	012	011	010	007	006	005	004	003	002	001	000	V40600
037	036	035	034	033	032	031	030	027	026	025	024	023	022	021	020	V40601
057	056	055	054	053	052	051	050	047	046	045	044	043	042	041	040	V40602
077	076	075	074	073	072	071	070	067	066	065	064	063	062	061	060	V40603
117	116	115	114	113	112	111	110	107	106	105	104	103	102	101	100	V40604
137	136	135	134	133	132	131	130	127	126	125	124	123	122	121	120	V40605
157	156	155	154	153	152	151	150	147	146	145	144	143	142	141	140	V40606
177	176	175	174	173	172	171	170	167	166	165	164	163	162	161	160	V40607
217	216	215	214	213	212	211	210	207	206	205	204	203	202	201	200	V40610
237	236	235	234	233	232	231	230	227	226	225	224	223	222	221	220	V40611
257	256	255	254	253	252	251	250	247	246	245	244	243	242	241	240	V40612
277	276	275	274	273	272	271	270	267	266	265	264	263	262	261	260	V40613
317	316	315	314	313	312	311	310	307	306	305	304	303	302	301	300	V40614
337	336	335	334	333	332	331	330	327	326	325	324	323	322	321	320	V40615
357	356	355	354	353	352	351	350	347	346	345	344	343	342	341	340	V40616
377	376	375	374	373	372	371	370	367	366	365	364	363	362	361	360	V40617

MSB	Additional DL250-1/DL260 Control Relays (C)															LSB	Address
417	416	415	414	413	412	411	410	407	406	405	404	403	402	401	400	V40620
437	436	435	434	433	432	431	430	427	426	425	424	423	422	421	420	V40621
457	456	455	454	453	452	451	450	447	446	445	444	443	442	441	440	V40622
477	476	475	474	473	472	471	470	467	466	465	464	463	462	461	460	V40623
517	516	515	514	513	512	511	510	507	506	505	504	503	502	501	500	V40624
537	536	535	534	533	532	531	530	527	526	525	524	523	522	521	520	V40625
557	556	555	554	553	552	551	550	547	546	545	544	543	542	541	540	V40626
577	576	575	574	573	572	571	570	567	566	565	564	563	562	561	560	V40627
617	616	615	614	613	612	611	610	607	606	605	604	603	602	601	600	V40630
637	636	635	634	633	632	631	630	627	626	625	624	623	622	621	620	V40631
657	656	655	654	653	652	651	650	647	646	645	644	643	642	641	640	V40632
677	676	675	674	673	672	671	670	667	666	665	664	663	662	661	660	V40633
717	716	715	714	713	712	711	710	707	706	705	704	703	702	701	700	V40634
737	736	735	734	733	732	731	730	727	726	725	724	723	722	721	720	V40635
757	756	755	754	753	752	751	750	747	746	745	744	743	742	741	740	V40636
777	776	775	774	773	772	771	770	767	766	765	764	763	762	761	760	V40637

MSB	Additional DL250-1/DL260 Control Relays (C)														LSB	Address
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1017	1016	1015	1014	1013	1012	1011	1010	1007	1006	1005	1004	1003	1002	1001	1000	**V40640**
1037	1036	1035	1034	1033	1032	1031	1030	1027	1026	1025	1024	1023	1022	1021	1020	**V40641**
1057	1056	1055	1054	1053	1052	1051	1050	1047	1046	1045	1044	1043	1042	1041	1040	**V40642**
1077	1076	1075	1074	1073	1072	1071	1070	1067	1066	1065	1064	1063	1062	1061	1060	**V40643**
1117	1116	1115	1114	1113	1112	1111	1110	1107	1106	1105	1104	1103	1102	1101	1100	**V40644**
1137	1136	1135	1134	1133	1132	1131	1130	1127	1126	1125	1124	1123	1122	1121	1120	**V40645**
1157	1156	1155	1154	1153	1152	1151	1150	1147	1146	1145	1144	1143	1142	1141	1140	**V40646**
1177	1176	1175	1174	1173	1172	1171	1170	1167	1166	1165	1164	1163	1162	1161	1160	**V40647**
1217	1216	1215	1214	1213	1212	1211	1210	1207	1206	1205	1204	1203	1202	1201	1200	**V40650**
1237	1236	1235	1234	1233	1232	1231	1230	1227	1226	1225	1224	1223	1222	1221	1220	**V40651**
1257	1256	1255	1254	1253	1252	1251	1250	1247	1246	1245	1244	1243	1242	1241	1240	**V40652**
1277	1276	1275	1274	1273	1272	1271	1270	1267	1266	1265	1264	1263	1262	1261	1260	**V40653**
1317	1316	1315	1314	1313	1312	1311	1310	1307	1306	1305	1304	1303	1302	1301	1300	**V40654**
1337	1336	1335	1334	1333	1332	1331	1330	1327	1326	1325	1324	1323	1322	1321	1320	**V40655**
1357	1356	1355	1354	1353	1352	1351	1350	1347	1346	1345	1344	1343	1342	1341	1340	**V40656**
1377	1376	1375	1374	1373	1372	1371	1370	1367	1366	1365	1364	1363	1362	1361	1360	**V40657**
1417	1416	1415	1414	1413	1412	1411	1410	1407	1406	1405	1404	1403	1402	1401	1400	**V40660**
1437	1436	1435	1434	1433	1432	1431	1430	1427	1426	1425	1424	1423	1422	1421	1420	**V40661**
1457	1456	1455	1454	1453	1452	1451	1450	1447	1446	1445	1444	1443	1442	1441	1440	**V40662**
1477	1476	1475	1474	1473	1472	1471	1470	1467	1466	1465	1464	1463	1462	1461	1460	**V40663**
1517	1516	1515	1514	1513	1512	1511	1510	1507	1506	1505	1504	1503	1502	1501	1500	**V40664**
1537	1536	1535	1534	1533	1532	1531	1530	1527	1526	1525	1524	1523	1522	1521	1520	**V40665**
1557	1556	1555	1554	1553	1552	1551	1550	1547	1546	1545	1544	1543	1542	1541	1540	**V40666**
1577	1576	1575	1574	1573	1572	1571	1570	1567	1566	1565	1564	1563	1562	1561	1560	**V40667**
1617	1616	1615	1614	1613	1612	1611	1610	1607	1606	1605	1604	1603	1602	1601	1600	**V40670**
1637	1636	1635	1634	1633	1632	1631	1630	1627	1626	1625	1624	1623	1622	1621	1620	**V40671**
1657	1656	1655	1654	1653	1652	1651	1650	1647	1646	1645	1644	1643	1642	1641	1640	**V40672**
1677	1676	1675	1674	1673	1672	1671	1670	1667	1666	1665	1664	1663	1662	1661	1660	**V40673**
1717	1716	1715	1714	1713	1712	1711	1710	1707	1706	1705	1704	1703	1702	1701	1700	**V40674**
1737	1736	1735	1734	1733	1732	1731	1730	1727	1726	1725	1724	1723	1722	1721	1720	**V40675**
1757	1756	1755	1754	1753	1752	1751	1750	1747	1746	1745	1744	1743	1742	1741	1740	**V40676**
1777	1776	1775	1774	1773	1772	1771	1770	1767	1766	1765	1764	1763	1762	1761	1760	**V40677**

This portion of the table shows additional Control Relays points available with the DL260.

MSB	Additional DL260 Control Relays (C)														LSB	Address
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
2017	2016	2015	2014	2013	2012	2011	2010	2007	2006	2005	2004	2003	2002	2001	2000	**V40700**
2037	2036	2035	2034	2033	2032	2031	2030	2027	2026	2025	2024	2023	2022	2021	2020	**V40701**
2057	2056	2055	2054	2053	2052	2051	2050	2047	2046	2045	2044	2043	2042	2041	2040	**V40702**
2077	2076	2075	2074	2073	2072	2071	2070	2067	2066	2065	2064	2063	2062	2061	2060	**V40703**
2117	2116	2115	2114	2113	2112	2111	2110	2107	2106	2105	2104	2103	2102	2101	2100	**V40704**
2137	2136	2135	2134	2133	2132	2131	2130	2127	2126	2125	2124	2123	2122	2121	2120	**V40705**
2157	2156	2155	2154	2153	2152	2151	2150	2147	2146	2145	2144	2143	2142	2141	2140	**V40706**
2177	2176	2175	2174	2173	2172	2171	2170	2167	2166	2165	2164	2163	2162	2161	2160	**V40707**
2217	2216	2215	2214	2213	2212	2211	2210	2207	2206	2205	2204	2203	2202	2201	2200	**V40710**
2237	2236	2235	2234	2233	2232	2231	2230	2227	2226	2225	2224	2223	2222	2221	2220	**V40711**
2257	2256	2255	2254	2253	2252	2251	2250	2247	2246	2245	2244	2243	2242	2241	2240	**V40712**
2277	2276	2275	2274	2273	2272	2271	2270	2267	2266	2265	2264	2263	2262	2261	2260	**V40713**
2317	2316	2315	2314	2313	2312	2311	2310	2307	2306	2305	2304	2303	2302	2301	2300	**V40714**
2337	2336	2335	2334	2333	2332	2331	2330	2327	2326	2325	2324	2323	2322	2321	2320	**V40715**
2357	2356	2355	2354	2353	2352	2351	2350	2347	2346	2345	2344	2343	2342	2341	2340	**V40716**
2377	2376	2375	2374	2373	2372	2371	2370	2367	2366	2365	2364	2363	2362	2361	2360	**V40717**
2417	2416	2415	2414	2413	2412	2411	2410	2407	2406	2405	2404	2403	2402	2401	2400	**V40720**
2437	2436	2435	2434	2433	2432	2431	2430	2427	2426	2425	2424	2423	2422	2421	2420	**V40721**
2457	2456	2455	2454	2453	2452	2451	2450	2447	2446	2445	2444	2443	2442	2441	2440	**V40722**
2477	2476	2475	2474	2473	2472	2471	2470	2467	2466	2465	2464	2463	2462	2461	2460	**V40723**
2517	2516	2515	2514	2513	2512	2511	2510	2507	2506	2505	2504	2503	2502	2501	2500	**V40724**
2537	2536	2535	2534	2533	2532	2531	2530	2527	2526	2525	2524	2523	2522	2521	2520	**V40725**
2557	2556	2555	2554	2553	2552	2551	2550	2547	2546	2545	2544	2543	2542	2541	2540	**V40726**
2577	2576	2575	2574	2573	2572	2571	2570	2567	2566	2565	2564	2563	2562	2561	2560	**V40727**
2617	2616	2615	2614	2613	2612	2611	2610	2607	2606	2605	2604	2603	2602	2601	2600	**V40730**
2637	2636	2635	2634	2633	2632	2631	2630	2627	2626	2625	2624	2623	2622	2621	2620	**V40731**
2657	2656	2655	2654	2653	2652	2651	2650	2647	2646	2645	2644	2643	2642	2641	2640	**V40732**
2677	2676	2675	2674	2673	2672	2671	2670	2667	2666	2665	2664	2663	2662	2661	2660	**V40733**
2717	2716	2715	2714	2713	2712	2711	2710	2707	2706	2705	2704	2703	2702	2701	2700	**V40734**
2737	2736	2735	2734	2733	2732	2731	2730	2727	2726	2725	2724	2723	2722	2721	2720	**V40735**
2757	2756	2755	2754	2753	2752	2751	2750	2747	2746	2745	2744	2743	2742	2741	2740	**V40736**
2777	2776	2775	2774	2773	2772	2771	2770	2767	2766	2765	2764	2763	2762	2761	2760	**V40737**

MSB	Additional DL260 Control Relays (C)														LSB	Address
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
3017	3016	3015	3014	3013	3012	3011	3010	3007	3006	3005	3004	3003	3002	3001	3000	**V40740**
3037	3036	3035	3034	3033	3032	3031	3030	3027	3026	3025	3024	3023	3022	3021	3020	**V40741**
3057	3056	3055	3054	3053	3052	3051	3050	3047	3046	3045	3044	3043	3042	3041	3040	**V40742**
3077	3076	3075	3074	3073	3072	3071	3070	3067	3066	3065	3064	3063	3062	3061	3060	**V40743**
3117	3116	3115	3114	3113	3112	3111	3110	3107	3106	3105	3104	3103	3102	3101	3100	**V40744**
3137	3136	3135	3134	3133	3132	3131	3130	3127	3126	3125	3124	3123	3122	3121	3120	**V40745**
3157	3156	3155	3154	3153	3152	3151	3150	3147	3146	3145	3144	3143	3142	3141	3140	**V40746**
3177	3176	3175	3174	3173	3172	3171	3170	3167	3166	3165	3164	3163	3162	3161	3160	**V40747**
3217	3216	3215	3214	3213	3212	3211	3210	3207	3206	3205	3204	3203	3202	3201	3200	**V40750**
3237	3236	3235	3234	3233	3232	3231	3230	3227	3226	3225	3224	3223	3222	3221	3220	**V40751**
3257	3256	3255	3254	3253	3252	3251	3250	3247	3246	3245	3244	3243	3242	3241	3240	**V40752**
3277	3276	3275	3274	3273	3272	3271	3270	3267	3266	3265	3264	3263	3262	3261	3260	**V40753**
3317	3316	3315	3314	3313	3312	3311	3310	3307	3306	3305	3304	3303	3302	3301	3300	**V40754**
3337	3336	3335	3334	3333	3332	3331	3330	3327	3326	3325	3324	3323	3322	3321	3320	**V40755**
3357	3356	3355	3354	3353	3352	3351	3350	3347	3346	3345	3344	3343	3342	3341	3340	**V40756**
3377	3376	3375	3374	3373	3372	3371	3370	3367	3366	3365	3364	3363	3362	3361	3360	**V40757**
3417	3416	3415	3414	3413	3412	3411	3410	3407	3406	3405	3404	3403	3402	3401	3400	**V40760**
3437	3436	3435	3434	3433	3432	3431	3430	3427	3426	3425	3424	3423	3422	3421	3420	**V40761**
3457	3456	3455	3454	3453	3452	3451	3450	3447	3446	3445	3444	3443	3442	3441	3440	**V40762**
3477	3476	3475	3474	3473	3472	3471	3470	3467	3466	3465	3464	3463	3462	3461	3460	**V40763**
3517	3516	3515	3514	3513	3512	3511	3510	3507	3506	3505	3504	3503	3502	3501	3500	**V40764**
3537	3536	3535	3534	3533	3532	3531	3530	3527	3526	3525	3524	3523	3522	3521	3520	**V40765**
3557	3556	3555	3554	3553	3552	3551	3550	3547	3546	3545	3544	3543	3542	3541	3540	**V40766**
3577	3576	3575	3574	3573	3572	3571	3570	3567	3566	3565	3564	3563	3562	3561	3560	**V40767**
3617	3616	3615	3614	3613	3612	3611	3610	3607	3606	3605	3604	3603	3602	3601	3600	**V40770**
3637	3636	3635	3634	3633	3632	3631	3630	3627	3626	3625	3624	3623	3622	3621	3620	**V40771**
3657	3656	3655	3654	3653	3652	3651	3650	3647	3646	3645	3644	3643	3642	3641	3640	**V40772**
3677	3676	3675	3674	3673	3672	3671	3670	3667	3666	3665	3664	3663	3662	3661	3660	**V40773**
3717	3716	3715	3714	3713	3712	3711	3710	3707	3706	3705	3704	3703	3702	3701	3700	**V40774**
3737	3736	3735	3734	3733	3732	3731	3730	3727	3726	3725	3724	3723	3722	3721	3720	**V40775**
3757	3756	3755	3754	3753	3752	3751	3750	3747	3746	3745	3744	3743	3742	3741	3740	**V40776**
3777	3776	3775	3774	3773	3772	3771	3770	3767	3766	3765	3764	3763	3762	3761	3760	**V40777**

Stage Control/Status Bit Map

This table provides a listing of the individual Stage control bits associated with each V-memory address.

MSB	DL230/DL240/DL250-1/DL260 Stage (S) Control Bits														LSB	Address
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
17	16	15	14	13	12	11	10	7	6	5	4	3	2	1	0	V41000
037	036	035	034	033	032	031	030	027	026	025	024	023	022	021	020	V41001
057	056	055	054	053	052	051	050	047	046	045	044	043	042	041	040	V41002
077	076	075	074	073	072	071	070	067	066	065	064	063	062	061	060	V41003
117	116	115	114	113	112	111	110	107	106	105	104	103	102	101	100	V41004
137	136	135	134	133	132	131	130	127	126	125	124	123	122	121	120	V41005
157	156	155	154	153	152	151	150	147	146	145	144	143	142	141	140	V41006
177	176	175	174	173	172	171	170	167	166	165	164	163	162	161	160	V41007
217	216	215	214	213	212	211	210	207	206	205	204	203	202	201	200	V41010
237	236	235	234	233	232	231	230	227	226	225	224	223	222	221	220	V41011
257	256	255	254	253	252	251	250	247	246	245	244	243	242	241	240	V41012
277	276	275	274	273	272	271	270	267	266	265	264	263	262	261	260	V41013
317	316	315	314	313	312	311	310	307	306	305	304	303	302	301	300	V41014
337	336	335	334	333	332	331	330	327	326	325	324	323	322	321	320	V41015
357	356	355	354	353	352	351	350	347	346	345	344	343	342	341	340	V41016
377	376	375	374	373	372	371	370	367	366	365	364	363	362	361	360	V41017

MSB	Additional DL240/DL250-1/DL260 Stage (S) Control Bits														LSB	Address
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
417	416	415	414	413	412	411	410	407	406	405	404	403	402	401	400	V41020
437	436	435	434	433	432	431	430	427	426	425	424	423	422	421	420	V41021
457	456	455	454	453	452	451	450	447	446	445	444	443	442	441	440	V41022
477	476	475	474	473	472	471	470	467	466	465	464	463	462	461	460	V41023
517	516	515	514	513	512	511	510	507	506	505	504	503	502	501	500	V41024
537	536	535	534	533	532	531	530	527	526	525	524	523	522	521	520	V41025
557	556	555	554	553	552	551	550	547	546	545	544	543	542	541	540	V41026
577	576	575	574	573	572	571	570	567	566	565	564	563	562	561	560	V41027
617	616	615	614	613	612	611	610	607	606	605	604	603	602	601	600	V41030
637	636	635	634	633	632	631	630	627	626	625	624	623	622	621	620	V41031
657	656	655	654	653	652	651	650	647	646	645	644	643	642	641	640	V41032
677	676	675	674	673	672	671	670	667	666	665	664	663	662	661	660	V41033
717	716	715	714	713	712	711	710	707	706	705	704	703	702	701	700	V41034
737	736	735	734	733	732	731	730	727	726	725	724	723	722	721	720	V41035
757	756	755	754	753	752	751	750	747	746	745	744	743	742	741	740	V41036
777	776	775	774	773	772	771	770	767	766	765	764	763	762	761	760	V41037

MSB	Additional DL250-1/DL260 Stage (S) Control Bits														LSB	Address
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1017	1016	1015	1014	1013	1012	1011	1010	1007	1006	1005	1004	1003	1002	1001	1000	**V41040**
1037	1036	1035	1034	1033	1032	1031	1030	1027	1026	1025	1024	1023	1022	1021	1020	**V41041**
1057	1056	1055	1054	1053	1052	1051	1050	1047	1046	1045	1044	1043	1042	1041	1040	**V41042**
1077	1076	1075	1074	1073	1072	1071	1070	1067	1066	1065	1064	1063	1062	1061	1060	**V41043**
1117	1116	1115	1114	1113	1112	1111	1110	1107	1106	1105	1104	1103	1102	1101	1100	**V41044**
1137	1136	1135	1134	1133	1132	1131	1130	1127	1126	1125	1124	1123	1122	1121	1120	**V41045**
1157	1156	1155	1154	1153	1152	1151	1150	1147	1146	1145	1144	1143	1142	1141	1140	**V41046**
1177	1176	1175	1174	1173	1172	1171	1170	1167	1166	1165	1164	1163	1162	1161	1160	**V41047**
1217	1216	1215	1214	1213	1212	1211	1210	1207	1206	1205	1204	1203	1202	1201	1200	**V41050**
1237	1236	1235	1234	1233	1232	1231	1230	1227	1226	1225	1224	1223	1222	1221	1220	**V41051**
1257	1256	1255	1254	1253	1252	1251	1250	1247	1246	1245	1244	1243	1242	1241	1240	**V41052**
1277	1276	1275	1274	1273	1272	1271	1270	1267	1266	1265	1264	1263	1262	1261	1260	**V41053**
1317	1316	1315	1314	1313	1312	1311	1310	1307	1306	1305	1304	1303	1302	1301	1300	**V41054**
1337	1336	1335	1334	1333	1332	1331	1330	1327	1326	1325	1324	1323	1322	1321	1320	**V41055**
1357	1356	1355	1354	1353	1352	1351	1350	1347	1346	1345	1344	1343	1342	1341	1340	**V41056**
1377	1376	1375	1374	1373	1372	1371	1370	1367	1366	1365	1364	1363	1362	1361	1360	**V41057**
1417	1416	1415	1414	1413	1412	1411	1410	1407	1406	1405	1404	1403	1402	1401	1400	**V41060**
1437	1436	1435	1434	1433	1432	1431	1430	1427	1426	1425	1424	1423	1422	1421	1420	**V41061**
1457	1456	1455	1454	1453	1452	1451	1450	1447	1446	1445	1444	1443	1442	1441	1440	**V41062**
1477	1476	1475	1474	1473	1472	1471	1470	1467	1466	1465	1464	1463	1462	1461	1460	**V41063**
1517	1516	1515	1514	1513	1512	1511	1510	1507	1506	1505	1504	1503	1502	1501	1500	**V41064**
1537	1536	1535	1534	1533	1532	1531	1530	1527	1526	1525	1524	1523	1522	1521	1520	**V41065**
1557	1556	1555	1554	1553	1552	1551	1550	1547	1546	1545	1544	1543	1542	1541	1540	**V41066**
1577	1576	1575	1574	1573	1572	1571	1570	1567	1566	1565	1564	1563	1562	1561	1560	**V41067**
1617	1616	1615	1614	1613	1612	1611	1610	1607	1606	1605	1604	1603	1602	1601	1600	**V41070**
1637	1636	1635	1634	1633	1632	1631	1630	1627	1626	1625	1624	1623	1622	1621	1620	**V41071**
1657	1656	1655	1654	1653	1652	1651	1650	1647	1646	1645	1644	1643	1642	1641	1640	**V41072**
1677	1676	1675	1674	1673	1672	1671	1670	1667	1666	1665	1664	1663	1662	1661	1660	**V41073**
1717	1716	1715	1714	1713	1712	1711	1710	1707	1706	1705	1704	1703	1702	1701	1700	**V41074**
1737	1736	1735	1734	1733	1732	1731	1730	1727	1726	1725	1724	1723	1722	1721	1720	**V41075**
1757	1756	1755	1754	1753	1752	1751	1750	1747	1746	1745	1744	1743	1742	1741	1740	**V41076**
1777	1776	1775	1774	1773	1772	1771	1770	1767	1766	1765	1764	1763	1762	1761	1760	**V41077**

Timer and Counter Status Bit Maps

This table provides a listing of the individual timer and counter contacts associated with each V-memory address bit.

MSB	DL230/DL240/DL250-1/DL260 Timer (T) and Counter (CT) Contacts															LSB	Timer	Counter
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		Address	Address
017	016	015	014	013	012	011	010	007	006	005	004	003	002	001	000		V41100	V41140
037	036	035	034	033	032	031	030	027	026	025	024	023	022	021	020		V41101	V41141
057	056	055	054	053	052	051	050	047	046	045	044	043	042	041	040		V41102	V41142
077	076	075	074	073	072	071	070	067	066	065	064	063	062	061	060		V41103	V41143

This portion of the table shows additional Timer and Counter contacts available with the DL240/250–1/260.

MSB	Additional DL240/DL250-1/DL260 Timer (T) and Counter (CT) Contacts															LSB	Timer	Counter
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		Address	Address
117	116	115	114	113	112	111	110	107	106	105	104	103	102	101	100		V41104	V41144
137	136	135	134	133	132	131	130	127	126	125	124	123	122	121	120		V41105	V41145
157	156	155	154	153	152	151	150	147	146	145	144	143	142	141	140		V41106	V41146
177	176	175	174	173	172	171	170	167	166	165	164	163	162	161	160		V41107	V41147

This portion of the table shows additional Timer contacts available with the DL250-1 and DL260.

MSB	Additional DL250-1/DL260 Timer (T) Contacts															LSB	Timer
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		Address
217	216	215	214	213	212	211	210	207	206	205	204	203	202	201	200		V41110
237	236	235	234	233	232	231	230	227	226	225	224	223	222	221	220		V41111
257	256	255	254	253	252	251	250	247	246	245	244	243	242	241	240		V41112
277	276	275	274	273	272	271	270	267	266	265	264	263	262	261	260		V41113
317	316	315	314	313	312	311	310	307	306	305	304	303	302	301	300		V41114
337	336	335	334	333	332	331	330	327	326	325	324	323	322	321	320		V41115
357	356	355	354	353	352	351	350	347	346	345	344	343	342	341	340		V41116
377	376	375	374	373	372	371	370	367	366	365	364	363	362	361	360		V41117

This portion of the table shows additional Counter contacts available with the DL260.

MSB	Additional DL260 Counter (CT) Contacts															LSB	Counter
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		Address
217	216	215	214	213	212	211	210	207	206	205	204	203	202	201	200		V41150
237	236	235	234	233	232	231	230	227	226	225	224	223	222	221	220		V41151
257	256	255	254	253	252	251	250	247	246	245	244	243	242	241	240		V41152
277	276	275	274	273	272	271	270	267	266	265	264	263	262	261	260		V41153
317	316	315	314	313	312	311	310	307	306	305	304	303	302	301	300		V41154
337	336	335	334	333	332	331	330	327	326	325	324	323	322	321	320		V41155
357	356	355	354	353	352	351	350	347	346	345	344	343	342	341	340		V41156
377	376	375	374	373	372	371	370	367	366	365	364	363	362	361	360		V41157

Remote I/O Bit Map

This table provides a listing of the individual remote I/O points associated with each V-memory address bit.

MSB	DL260 Remote I/O (GX) and (GY) Points														LSB	GX	GY
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Address
017	016	015	014	013	012	011	010	007	006	005	004	003	002	001	000	**V40000**	**V40200**
037	036	035	034	033	032	031	030	027	026	025	024	023	022	021	020	**V40001**	**V40201**
057	056	055	054	053	052	051	050	047	046	045	044	043	042	041	040	**V40002**	**V40202**
077	076	075	074	073	072	071	070	067	066	065	064	063	062	061	060	**V40003**	**V40203**
117	116	115	114	113	112	111	110	107	106	105	104	103	102	101	100	**V40004**	**V40204**
137	136	135	134	133	132	131	130	127	126	125	124	123	122	121	120	**V40005**	**V40205**
157	156	155	154	153	152	151	150	147	146	145	144	143	142	141	140	**V40006**	**V40206**
177	176	175	174	173	172	171	170	167	166	165	164	163	162	161	160	**V40007**	**V40207**
217	216	215	214	213	212	211	210	207	206	205	204	203	202	201	200	**V40010**	**V40210**
237	236	235	234	233	232	231	230	227	226	225	224	223	222	221	220	**V40011**	**V40211**
257	256	255	254	253	252	251	250	247	246	245	244	243	242	241	240	**V40012**	**V40212**
277	276	275	274	273	272	271	270	267	266	265	264	263	262	261	260	**V40013**	**V40213**
317	316	315	314	313	312	311	310	307	306	305	304	303	302	301	300	**V40004**	**V40214**
337	336	335	334	333	332	331	330	327	326	325	324	323	322	321	320	**V40015**	**V40215**
357	356	355	354	353	352	351	350	347	346	345	344	343	342	341	340	**V40016**	**V40216**
377	376	375	374	373	372	371	370	367	366	365	364	363	362	361	360	**V40007**	**V40217**
417	416	415	414	413	412	411	410	407	406	405	404	403	402	401	400	**V40020**	**V40220**
437	436	435	434	433	432	431	430	427	426	425	424	423	422	421	420	**V40021**	**V40221**
457	456	455	454	453	452	451	450	447	446	445	444	443	442	441	440	**V40022**	**V40222**
477	476	475	474	473	472	471	470	467	466	465	464	463	462	461	460	**V40023**	**V40223**
517	516	515	514	513	512	511	510	507	506	505	504	503	502	501	500	**V40024**	**V40224**
537	536	535	534	533	532	531	530	527	526	525	524	523	522	521	520	**V40025**	**V40225**
557	556	555	554	553	552	551	550	547	546	545	544	543	542	541	540	**V40026**	**V40226**
577	576	575	574	573	572	571	570	567	566	565	564	563	562	561	560	**V40027**	**V40227**
617	616	615	614	613	612	611	610	607	606	605	604	603	602	601	600	**V40030**	**V40230**
637	636	635	634	633	632	631	630	627	626	625	624	623	622	621	620	**V40031**	**V40231**
657	656	655	654	653	652	651	650	647	646	645	644	643	642	641	640	**V40032**	**V40232**
677	676	675	674	673	672	671	670	667	666	665	664	663	662	661	660	**V40033**	**V40233**
717	716	715	714	713	712	711	710	707	706	705	704	703	702	701	700	**V40034**	**V40234**
737	736	735	734	733	732	731	730	727	726	725	724	723	722	721	720	**V40035**	**V40235**
757	756	755	754	753	752	751	750	747	746	745	744	743	742	741	740	**V40036**	**V40236**
777	776	775	774	773	772	771	770	767	766	765	764	763	762	761	760	**V40037**	**V40237**

MSB	DL260 Remote I/O (GX) and (GY) Points															LSB	GX	GY
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Address
1017	1016	1015	1014	1013	1012	1011	1010	1007	1006	1005	1004	1003	1002	1001	1000	V40040	V40240
1037	1036	1035	1034	1033	1032	1031	1030	1027	1026	1025	1024	1023	1022	1021	1020	V40041	V40241
1057	1056	1055	1054	1053	1052	1051	1050	1047	1046	1045	1044	1043	1042	1041	1040	V40042	V40242
1077	1076	1075	1074	1073	1072	1071	1070	1067	1066	1065	1064	1063	1062	1061	1060	V40043	V40243
1117	1116	1115	1114	1113	1112	1111	1110	1107	1106	1105	1104	1103	1102	1101	1100	V40044	V40244
1137	1136	1135	1134	1133	1132	1131	1130	1127	1126	1125	1124	1123	1122	1121	1120	V40045	V40245
1157	1156	1155	1154	1153	1152	1151	1150	1147	1146	1145	1144	1143	1142	1141	1140	V40046	V40246
1177	1176	1175	1174	1173	1172	1171	1170	1167	1166	1165	1164	1163	1162	1161	1160	V40047	V40247
1217	1216	1215	1214	1213	1212	1211	1210	1207	1206	1205	1204	1203	1202	1201	1200	V40050	V40250
1237	1236	1235	1234	1233	1232	1231	1230	1227	1226	1225	1224	1223	1222	1221	1220	V40051	V40251
1257	1256	1255	1254	1253	1252	1251	1250	1247	1246	1245	1244	1243	1242	1241	1240	V40052	V40252
1277	1276	1275	1274	1273	1272	1271	1270	1267	1266	1265	1264	1263	1262	1261	1260	V40053	V40253
1317	1316	1315	1314	1313	1312	1311	1310	1307	1306	1305	1304	1303	1302	1301	1300	V40054	V40254
1337	1336	1335	1334	1333	1332	1331	1330	1327	1326	1325	1324	1323	1322	1321	1320	V40055	V40255
1357	1356	1355	1354	1353	1352	1351	1350	1347	1346	1345	1344	1343	1342	1341	1340	V40056	V40256
1377	1376	1375	1374	1373	1372	1371	1370	1367	1366	1365	1364	1363	1362	1361	1360	V40057	V40257
1417	1416	1415	1414	1413	1412	1411	1410	1407	1406	1405	1404	1403	1402	1401	1400	V40060	V40260
1437	1436	1435	1434	1433	1432	1431	1430	1427	1426	1425	1424	1423	1422	1421	1420	V40061	V40261
1457	1456	1455	1454	1453	1452	1451	1450	1447	1446	1445	1444	1443	1442	1441	1440	V40062	V40262
1477	1476	1475	1474	1473	1472	1471	1470	1467	1466	1465	1464	1463	1462	1461	1460	V40063	V40263
1517	1516	1515	1514	1513	1512	1511	1510	1507	1506	1505	1504	1503	1502	1501	1500	V40064	V40264
1537	1536	1535	1534	1533	1532	1531	1530	1527	1526	1525	1524	1523	1522	1521	1520	V40065	V40265
1557	1556	1555	1554	1553	1552	1551	1550	1547	1546	1545	1544	1543	1542	1541	1540	V40066	V40266
1577	1576	1575	1574	1573	1572	1571	1570	1567	1566	1565	1564	1563	1562	1561	1560	V40067	V40267
1617	1616	1615	1614	1613	1612	1611	1610	1607	1606	1605	1604	1603	1602	1601	1600	V40070	V40270
1637	1636	1635	1634	1633	1632	1631	1630	1627	1626	1625	1624	1623	1622	1621	1620	V40071	V40271
1657	1656	1655	1654	1653	1652	1651	1650	1647	1646	1645	1644	1643	1642	1641	1640	V40072	V40272
1677	1676	1675	1674	1673	1672	1671	1670	1667	1666	1665	1664	1663	1662	1661	1660	V40073	V40273
1717	1716	1715	1714	1713	1712	1711	1710	1707	1706	1705	1704	1703	1702	1701	1700	V40074	V40274
1737	1736	1735	1734	1733	1732	1731	1730	1727	1726	1725	1724	1723	1722	1721	1720	V40075	V40275
1757	1756	1755	1754	1753	1752	1751	1750	1747	1746	1745	1744	1743	1742	1741	1740	V40076	V40276
1777	1776	1775	1774	1773	1772	1771	1770	1767	1766	1765	1764	1763	1762	1761	1760	V40077	V40277

MSB	DL260 Remote I/O (GX) and (GY) Points															LSB	GX	GY
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Address
2017	2016	2015	2014	2013	2012	2011	2010	2007	2006	2005	2004	2003	2002	2001	2000	**V40100**	**V40300**
2037	2036	2035	2034	2033	2032	2031	2030	2027	2026	2025	2024	2023	2022	2021	2020	**V40101**	**V40301**
2057	2056	2055	2054	2053	2052	2051	2050	2047	2046	2045	2044	2043	2042	2041	2040	**V40102**	**V40302**
2077	2076	2075	2074	2073	2072	2071	2070	2067	2066	2065	2064	2063	2062	2061	2060	**V40103**	**V40303**
2117	2116	2115	2114	2113	2112	2111	2110	2107	2106	2105	2104	2103	2102	2101	2100	**V40104**	**V40304**
2137	2136	2135	2134	2133	2132	2131	2130	2127	2126	2125	2124	2123	2122	2121	2120	**V40105**	**V40305**
2157	2156	2155	2154	2153	2152	2151	2150	2147	2146	2145	2144	2143	2142	2141	2140	**V40106**	**V40306**
2177	2176	2175	2174	2173	2172	2171	2170	2167	2166	2165	2164	2163	2162	2161	2160	**V40107**	**V40307**
2217	2216	2215	2214	2213	2212	2211	2210	2207	2206	2205	2204	2203	2202	2201	2200	**V40110**	**V40310**
2237	2236	2235	2234	2233	2232	2231	2230	2227	2226	2225	2224	2223	2222	2221	2220	**V40111**	**V40311**
2257	2256	2255	2254	2253	2252	2251	2250	2247	2246	2245	2244	2243	2242	2241	2240	**V40112**	**V40312**
2277	2276	2275	2274	2273	2272	2271	2270	2267	2266	2265	2264	2263	2262	2261	2260	**V40113**	**V40313**
2317	2316	2315	2314	2313	2312	2311	2310	2307	2306	2305	2304	2303	2302	2301	2300	**V40114**	**V40314**
2337	2336	2335	2334	2333	2332	2331	2330	2327	2326	2325	2324	2323	2322	2321	2320	**V40115**	**V40315**
2357	2356	2355	2354	2353	2352	2351	2350	2347	2346	2345	2344	2343	2342	2341	2340	**V40116**	**V40316**
2377	2376	2375	2374	2373	2372	2371	2370	2367	2366	2365	2364	2363	2362	2361	2360	**V40117**	**V40317**
2417	2416	2415	2414	2413	2412	2411	2410	2407	2406	2405	2404	2403	2402	2401	2400	**V40120**	**V40320**
2437	2436	2435	2434	2433	2432	2431	2430	2427	2426	2425	2424	2423	2422	2421	2420	**V40121**	**V40321**
2457	2456	2455	2454	2453	2452	2451	2450	2447	2446	2445	2444	2443	2442	2441	2440	**V40122**	**V40322**
2477	2476	2475	2474	2473	2472	2471	2470	2467	2466	2465	2464	2463	2462	2461	2460	**V40123**	**V40323**
2517	2516	2515	2514	2513	2512	2511	2510	2507	2506	2505	2504	2503	2502	2501	2500	**V40124**	**V40324**
2537	2536	2535	2534	2533	2532	2531	2530	2527	2526	2525	2524	2523	2522	2521	2520	**V40125**	**V40325**
2557	2556	2555	2554	2553	2552	2551	2550	2547	2546	2545	2544	2543	2542	2541	2540	**V40126**	**V40326**
2577	2576	2575	2574	2573	2572	2571	2570	2567	2566	2565	2564	2563	2562	2561	2560	**V40127**	**V40327**
2617	2616	2615	2614	2613	2612	2611	2610	2607	2606	2605	2604	2603	2602	2601	2600	**V40130**	**V40330**
2637	2636	2635	2634	2633	2632	2631	2630	2627	2626	2625	2624	2623	2622	2621	2620	**V40131**	**V40331**
2657	2656	2655	2654	2653	2652	2651	2650	2647	2646	2645	2644	2643	2642	2641	2640	**V40132**	**V40332**
2677	2676	2675	2674	2673	2672	2671	2670	2667	2666	2665	2664	2663	2662	2661	2660	**V40133**	**V40333**
2717	2716	2715	2714	2713	2712	2711	2710	2707	2706	2705	2704	2703	2702	2701	2700	**V40134**	**V40334**
2737	2736	2735	2734	2733	2732	2731	2730	2727	2726	2725	2724	2723	2722	2721	2720	**V40135**	**V40335**
2757	2756	2755	2754	2753	2752	2751	2750	2747	2736	2735	2734	2733	2732	2731	2730	**V40136**	**V40336**
2777	2776	2775	2774	2773	2772	2771	2770	2767	2766	2765	2764	2763	2762	2761	2760	**V40137**	**V40337**

MSB	DL260 Remote I/O (GX) and (GY) Points															LSB	GX	GY
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Address
3017	3016	3015	3014	3013	3012	3011	3010	3007	3006	3005	3004	3003	3002	3001	3000	**V40140**	**V40340**
3037	3036	3035	3034	3033	3032	3031	3030	3027	3026	3025	3024	3023	3022	3021	3020	**V40141**	**V40341**
3057	3056	3055	3054	3053	3052	3051	3050	3047	3046	3045	3044	3043	3042	3041	3040	**V40142**	**V40342**
3077	3076	3075	3074	3073	3072	3071	3070	3067	3066	3065	3064	3063	3062	3061	3060	**V40143**	**V40343**
3117	3116	3115	3114	3113	3112	3111	3110	3107	3106	3105	3104	3103	3102	3101	3100	**V40144**	**V40344**
3137	3136	3135	3134	3133	3132	3131	3130	3127	3126	3125	3124	3123	3122	3121	3120	**V40145**	**V40345**
3157	3156	3155	3154	3153	3152	3151	3150	3147	3146	3145	3144	3143	3142	3141	3140	**V40146**	**V40346**
3177	3176	3175	3174	3173	3172	3171	3170	3167	3166	3165	3164	3163	3162	3161	3160	**V40147**	**V40347**
3217	3216	3215	3214	3213	3212	3211	3210	3207	3206	3205	3204	3203	3202	3201	3200	**V40150**	**V40350**
3237	3236	3235	3234	3233	3232	3231	3230	3227	3226	3225	3224	3223	3222	3221	3220	**V40151**	**V40351**
3257	3256	3255	3254	3253	3252	3251	3250	3247	3246	3245	3244	3243	3242	3241	3240	**V40152**	**V40352**
3277	3276	3275	3274	3273	3272	3271	3270	3267	3266	3265	3264	3263	3262	3261	3260	**V40153**	**V40353**
3317	3316	3315	3314	3313	3312	3311	3310	3307	3306	3305	3304	3303	3302	3301	3300	**V40154**	**V40354**
3337	3336	3335	3334	3333	3332	3331	3330	3327	3326	3325	3324	3323	3322	3321	3320	**V40155**	**V40355**
3357	3356	3355	3354	3353	3352	3351	3350	3347	3346	3345	3344	3343	3342	3341	3340	**V40156**	**V40356**
3377	3376	3375	3374	3373	3372	3371	3370	3367	3366	3365	3364	3363	3362	3361	3360	**V40157**	**V40357**
3417	3416	3415	3414	3413	3412	3411	3410	3407	3406	3405	3404	3403	3402	3401	3400	**V40160**	**V40360**
3437	3436	3435	3434	3433	3432	3431	3430	3427	3426	3425	3424	3423	3422	3421	3420	**V40161**	**V40361**
3457	3456	3455	3454	3453	3452	3451	3450	3447	3446	3445	3444	3443	3442	3441	3440	**V40162**	**V40362**
3477	3476	3475	3474	3473	3472	3471	3470	3467	3466	3465	3464	3463	3462	3461	3460	**V40163**	**V40363**
3517	3516	3515	3514	3513	3512	3511	3510	3507	3506	3505	3504	3503	3502	3501	3500	**V40164**	**V40364**
3537	3536	3535	3534	3533	3532	3531	3530	3527	3526	3525	3524	3523	3522	3521	3520	**V40165**	**V40365**
3557	3556	3555	3554	3553	3552	3551	3550	3547	3546	3545	3544	3543	3542	3541	3540	**V40166**	**V40366**
3577	3576	3575	3574	3573	3572	3571	3570	3567	3566	3565	3564	3563	3562	3561	3560	**V40167**	**V40367**
3617	3616	3615	3614	3613	3612	3611	3610	3607	3606	3605	3604	3603	3602	3601	3600	**V40170**	**V40370**
3637	3636	3635	3634	3633	3632	3631	3630	3627	3626	3625	3624	3623	3622	3621	3620	**V40171**	**V40371**
3657	3656	3655	3654	3653	3652	3651	3650	3647	3646	3645	3644	3643	3642	3641	3640	**V40172**	**V40372**
3677	3676	3675	3674	3673	3672	3671	3670	3667	3666	3665	3664	3663	3662	3661	3660	**V40173**	**V40373**
3717	3716	3715	3714	3713	3712	3711	3710	3707	3706	3705	3704	3703	3702	3701	3700	**V40174**	**V40374**
3737	3736	3735	3734	3733	3732	3731	3730	3727	3726	3725	3724	3723	3722	3721	3720	**V40175**	**V40375**
3757	3756	3755	3754	3753	3752	3751	3750	3747	3746	3745	3744	3743	3742	3741	3740	**V40176**	**V40376**
3777	3776	3775	3774	3773	3772	3771	3770	3767	3766	3765	3764	3763	3762	3761	3760	**V40177**	**V40377**

Notes