Index



A

Accumulating Fast Timer instruction, 5–30
Accumulating Timer instruction, 5–30
Add Double instruction, 5–61
Add instruction, 5–60
Agency approvals, 2–9
And Double instruction, 5–53
And If Equal instruction, 5–19
And If Not Equal instruction, 5–19
And Immediate instruction, 5–24
And instruction, 5–11, 5–22, 5–52
And Not Immediate instruction, 5–24
And Not instruction, 5–11, 5–17
And Store instruction, 5–12
ASCII Constant instruction, 5–84
Auxiliary functions, 4–8, A–2

B

BCD numbers, 4-21
Binary Coded Decimal instruction, 5-72
Binary instruction, 5-71

C

Cables

operator interfaces, 2–17 programming, 1–11 programming devices, 2–17, 4–5 Common terminals, 2–19 Communications port, 4–4

Compare instruction, 5–58

Connectors
common terminals, 2–19
removal, 2–6

Counter instruction, 5–33

CPU
configuration, A–5
indicators, 8–6
instruction list, 5–2
memory map, 4–22
modes, 4–6

CPU specifications, 4–3

D

Data Label instruction, 5-84 Diagnostics, 4-14, 8-2 DIN rail mounting, 2-10 Disable Interrupts instruction, 5-80 Divide instruction, 5-65 DL105 Micro PLC front panel, 2-5 mounting guidelines, 2-7 DL105 Aliases, 4-28 Drum instruction, 6-2 drum control techniques, 6-10 EDRUM (Event Drum), 6-12 handheld programmer mnemonics, 6-14 overview of drum operation, 6-8 step transition, 6-4 Drum sequencer programming, 1-11

E

Emergency stop, 2-3

Index-2

Enable Interrupts instruction, 5-80	Instructions
Encode instruction, 5-69	accumulator / stack Load, 5-40
Encoder signals, 3-17	bit operations, 5-67 boolean, 5-3, 5-9
End instruction, 5–3	comparative boolean, 5-17
·	drum, 6–2
Environmental specifications, 2-9	execution times, 4-19, C-2
Equal relays, 3-9, D-3	immediate, 5-23
Error codes code locations, 8-3 listing, B-2 pulse output errors, 3-41	interrupt, 5-80 list of, 5-2 logical, 5-52 math, 5-60 message, 5-83
Exclusive Or Double instruction, 5-57	number conversions, 5-71
Exclusive Or instruction, 5-56	program control, 5-78 program control instructions, 4-19 stage, 7-19 stage programming, 7-2
•	table, 5-74
Fault instruction, 5-83	timer, counter, and shift register, 5-27
Forced I/O, 4-13	Interrupt instruction, 5-80
	Interrupt Return instruction, 5-80
Handheld programmer, A-6 EEPROM operations, A-7	Interrupts external, 3-45 HSIO input, 3-43 timed, 3-45
Hexadecimal numbers, 4-21	
High-speed I/O	J
discrete inputs with filter, 3-51 features, 3-2 high-speed counter, 3-6	Jump instruction, 7-7, 7-20
high-speed interrupts, 3-43 modes, 3-4 pulse catch input, 3-48	L
pulse output, 3-23	Load Address instruction, 5-48
quadrature counter, 3-17	Load Double instruction, 5-46
Home search profile, 3-36	Load instruction, 5-45
	Load Label instruction, 5-75
1	
•	M
I/O response time, 4-15	IVI
I/O Type Selection, 1-5	Maintenance, 8-2
Initial Stage instruction, 7-20	Manual, organization, 1-2
Initial Stages, 7-5	Master Line Reset instruction, 5-78
Input simulator, 1-7, 2-28	Master Line Set instruction, 5-78
Installation	Memory map, 4-22, 4-26
grounding, 2-8	Message instructions, 5-83
panel design specifications, 2-8	Motion control profile, 3-23

Mounting, Guidelines, 2-7 Program mode, 4-12 Move instruction, 5-74 Programming, concepts, 1-11 Move Memory Cartridge instruction, 5-75 Programming methods, 1-8 Multiply instruction, 5-64 Q N Quadrature counter, 3-17 Numbering Systems Quick start, 1-6 BCD, G-5 Binary, G-2 R Floating Point, G-6 Hexadecimal, G-3 Octal, G-4 Registration profile, 3-29, 3-33 Numerical Constant instruction, 5-84 Relay wiring, 2-22, 2-24 Reset instruction, 5-15 Retentive memory, 4-9 Run mode, 4-12 Octal numbers, 4-20, 4-22 Run time edits, 8-14 Or Double instruction, 5-55 Or If Equal instruction, 5-18 S Or If Not Equal instruction, 5-18 Or Immediate instruction, 5-23 Safety, panel design specifications, 2-4 Or instruction, 5-10, 5-21, 5-54 Safety guidelines, 2-2 Or Not Immediate instruction, 5-23 Scan time, 4-18 Or Not instruction, 5-10, 5-21 Scratchpad memory, 1-9, 4-9 Or Out Immediate instruction, 5-25 Set instruction, 5-15 Or Store instruction, 5-12 Shift Left instruction, 5-67 Out Double instruction, 5-49 Shift Right instruction, 5-68 Out Formatted instruction, 5-50 Sinking / sourcing I/O, 2-20 Out instruction, 5-49 Special relays, 4-13, 4-25, D-2, E-2 **Specifications** CPU, 4-3 P environmental, 2-9 F1-130AA, 2-38 Panel layout, 2-8 F1-130AD, 2-34 Part Numbers, 1-5 F1-130DA, 2-40 F1-130DD, 2-36 Password, 4-10, A-8 F1-130DD-D, 2-44 Pause instruction, 5-16 F1-130DR, 2-32 F1-130DR-D, 2-42 Pop instruction, 5-50 motion profiles, 3-26 Positive Differential instruction, 5-15 panel design, 2-8 Power wiring, 1-8 Stack, 5-7 Presets, 3-8, 3-10 Stage Counter instruction, 5-35 Program control instructions, 5-78 Stage instructions, 7-19

Index-4

Stage programming, 1-11, 7-2 four steps to writing a stage program, 7-9 garage door opener example, 7-10 initial stages, 7-5 introduction, 7-2 jump instruction, 7-7 mutually exclusive transitions, 7-14 parallel processes, 7-12 power flow transition, 7-18 program organization, 7-15 questions and answers, 7-21 stage data type, 4-25 stage instruction characteristics, 7-6 stage view, 7-18 state transition diagrams, 7-3 supervisor process, 7-17 timer inside stage, 7-13 Standard RLL Programming, 1-11 Store If Equal instruction, 5-17 Store If Not Equal instruction, 5-17 Store immediate instruction, 5-23 Store instruction, 5-9, 5-20 Store Not Immediate instruction, 5-23 Store Not instruction, 5-9, 5-20 Subtract double instruction, 5-63 Subtract instruction, 5-62 System, panel design specifications, 2-4 System design steps, 1-10 Table instructions, 5-74 Technical support, 1-2, 1-4 Trapezoidal profile, 3-30 Troubleshooting, 8-2 Troubleshooting, 8-2 counter input, 3-7 electrical noise, 8-10 error codes, B-2 !/O points, 8-8 program debug, 8-11 Troubleshooting guide HSIO Mode 10, 3-16 HSIO Mode 20, 3-22 HSIO Mode 30, 3-41

U

Up Down Counter instruction, 5-37



V-memory, 4-22, 4-26 Velocity profile, 3-29, 3-38

W

Wiring

counter input, 3-7
DC inputs, 2-25
DC outputs, 2-26
encoder, 3-18
high-speed I/O, 2-27
input simulator, 1-7, 2-28
power input, 1-7, 2-11, 2-14
pulse output, 3-25
relay outputs, 2-22

Wiring Guidelines, 2-11, 2-14