C

Instruction Execution Times

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— Introduction

— Instruction Execution Times

Introduction

This appendix contains several tables that provide the instruction execution times for DL105 Micro PLCs. Many of the execution times depend on the type of data used with the instruction. Registers may be classified into the following types:

- Data (word) Registers
- Bit Registers

V-Memory Data Registers

Some V-memory locations are considered data registers, such as timer or counter current values. Standard user V-memory is classified as a V-memory data register. Note that you can load a bit pattern into these types of registers, even though their primary use is for data registers. The following locations are data registers:

Data Registers	DL105
Timer Current Values	V0 – V77
Counter Current Values	V1000 – V1077
User Data Words	V2000 – V2377 V4000 – V4177

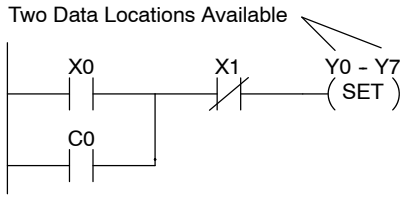
V-Memory Bit Registers

You may recall that some of the discrete points such as X, Y, C, etc. are automatically mapped into V-memory (see Appendix E). The following bit registers contain this data:

Bit Registers	DL105
Input Points (X)	V40400 – V 40407
Output Points (Y)	V40500 – V40507
Control Relays (C)	V40600 – V40617
Timer Status Bits	V41100 – V41103
Counter Status Bits	V41140 – V41143
Stages	V41000 – V41017

How to Read the Tables

Some instructions can have more than one parameter. For example, the SET instruction shown in the ladder program to the right can set a single point or a range of points.



In these cases, execution times that depend on the amount and type of parameters. The execution time tables list execution times for both situations, as shown below:

SET	1st #:	X, Y, C, S		17.4 µs
	2nd #:	X, Y, C, S,	(N pt)	12.0µs+5.4µsxN
RST	1st #:	X, Y, C, S		19.5 µs
	2nd #:	X, Y, C, S,	(N pt)	10.5µs+5.2µsxN

Execution depends on numbers of locations and types of data used

Instruction Execution Times

Boolean Instructions

Boolean Instructions		DL105	
Instruction	**Legal Data Types**	**Execute**	**Not Execute**
STR	X, Y, C, T, CT,S, SP	3.3 µs	3.3 µs
STRN	X, Y, C, T, CT,S, SP	3.9 µs	3.9 µs
OR	X, Y, C, T, CT, S, SP	2.7 µs	2.7 µs
ORN	X, Y, C, T, CT,S, SP	3.3 µs	3.3 µs
AND	X, Y, C, T, CT, S, SP	2.1 µs	2.1 µs
ANDN	X, Y, C, T, CT, S, SP	2.7 µs	2.7 µs
ANDSTR	None	1.2 µs	1.2 µs
ORSTR	None	1.2 µs	1.2 µs
OUT	X, Y, C	3.4 µs	3.4 µs
OROUT	X, Y, C	8.6 µs	8.6 µs
PD	X, Y, C	13.5 µs	13.5 µs
SET	1st #: X, Y, C, S 2nd #: X, Y, C, S (N pt)	17.4 µs 12.0µs+5.4µsxN	6.8 µs 6.8 µs
RST	1st #: T, CT 2nd #: T, CT (N pt)	31.6 µs 17µs+14.6µsxN	6.8 µs 6.8 µs
PAUSE	1wd: Y 2wd: Y (N points)	19.0 µs 15µs+4µs x N	19.0 µs 15µs+4µs x N
RST	1st #: X, Y, C, S 2nd #: X, Y, C, S (N pt)	17.7 µs 10.5µs+5.2µsxN	6.8 µs 6.8 µs

Comparative Boolean Instructions

Comparative Boolean Instructions			DL105	
Instruction	**Legal Data Types**		**Execute**	**Not Execute**
STRE	1st	2nd		
	V: Data Reg.	V:Data Reg. V:Bit Reg. K:Constant	77 µs 158 µs 57 µs	13.8 µs 13.8 µs 13.8 µs
	V: Bit Reg.	V:Data Reg. V:Bit Reg. K:Constant	158 µs 240 µs 139 µs	13.8 µs 13.8 µs 13.8 µs
STRNE	1st	2nd		
	V: Data Reg.	V:Data Reg. V:Bit Reg. K:Constant	77 µs 158 µs 57 µs	13.8 µs 13.8 µs 13.8 µs
	V: Bit Reg.	V:Data Reg. V:Bit Reg. K:Constant	158 µs 240 µs 139 µs	13.8 µs 13.8 µs 13.8 µs

Comparative Boolean (cont.)			DL105	
Instruction	**Legal Data Types**		**Execute**	**Not Execute**
ORE	1st	2nd		
	V: Data Reg.	V:Data Reg. V:Bit Reg. K:Constant	75 µs 158 µs 55 µs	12.0 µs 12.0 µs 12.0 µs
	V: Bit Reg.	V:Data Reg. V:Bit Reg. K:Constant	158 µs 239 µs 137 µs	12.0 µs 12.0 µs 12.0 µs
ORNE	1st	2nd		
	V: Data Reg.	V:Data Reg. V:Bit Reg. K:Constant	75 µs 158 µs 55 µs	12.0 µs 12.0 µs 12.0 µs
	V: Bit Reg.	V:Data Reg. V:Bit Reg. K:Constant	158 µs 239 µs 137 µs	12.0 µs 12.0 µs 12.0 µs
ANDE	1st	2nd		
	V: Data Reg.	V:Data Reg. V:Bit Reg. K:Constant	75 µs 158 µs 55 µs	12.0 µs 12.0 µs 12.0 µs
	V: Bit Reg.	V:Data Reg. V:Bit Reg. K:Constant	158 µs 239 µs 137 µs	12.0 µs 12.0 µs 12.0 µs
ANDNE	1st	2nd		
	V: Data Reg.	V:Data Reg. V:Bit Reg. K:Constant	75 µs 158 µs 55 µs	12.0 µs 12.0 µs 12.0 µs
	V: Bit Reg.	V:Data Reg. V:Bit Reg. K:Constant	158 µs 239 µs 137 µs	12.0 µs 12.0 µs 12.0 µs
STR	1st	2nd		
	T, CT	V:Data Reg. V:Bit Reg. K:Constant	78 µs 158 µs 57 µs	13.8 µs 13.8 µs 13.8 µs
	1st	2nd		
	V: Data Reg.	V:Data Reg. V:Bit Reg. K:Constant	78 µs 159 µs 57 µs	13.8 µs 13.8 µs 13.8 µs
	V: Bit Reg.	V:Data Reg. V:Bit Reg. K:Constant	159 µs 241 µs 139 µs	13.8 µs 13.8 µs 13.8 µs
STRN	1st	2nd		
	T, CT	V:Data Reg. V:Bit Reg. K:Constant	78 µs 158 µs 57 µs	13.8 µs 13.8 µs 13.8 µs
	1st	2nd		
	V: Data Reg.	V:Data Reg. V:Bit Reg. K:Constant	78 µs 159 µs 57 µs	13.8 µs 13.8 µs 13.8 µs
	V: Bit Reg.	V:Data Reg. V:Bit Reg. K:Constant	159 µs 241 µs 139 µs	13.8 µs 13.8 µs 13.8 µs

Comparative Boolean (cont.)			DL105	
Instruction	**Legal Data Types**		**Execute**	**Not Execute**
OR	1st	2nd		
	T, CT	V:Data Reg. V:Bit Reg. K:Constant	75 µs 158 µs 55 µs	12.0 µs 12.0 µs 12.0 µs
	1st	2nd		
	V: Data Reg.	V:Data Reg. V:Bit Reg. K:Constant	75 µs 158 µs 55 µs	12.0 µs 12.0 µs 12.0 µs
	V: Bit Reg.	V:Data Reg. V:Bit Reg. K:Constant	158 µs 240 µs 137 µs	12.0 µs 12.0 µs 12.0 µs
ORN	1st	2nd		
	T, CT	V:Data Reg. V:Bit Reg. K:Constant	75 µs 158 µs 55 µs	12.0 µs 12.0 µs 12.0 µs
	1st	2nd		
	V: Data Reg.	V:Data Reg. V:Bit Reg. K:Constant	75 µs 158 µs 55 µs	12.0 µs 12.0 µs 12.0 µs
	V: Bit Reg.	V:Data Reg. V:Bit Reg. K:Constant	158 µs 240 µs 137 µs	12.0 µs 12.0 µs 12.0 µs
AND	1st	2nd		
	T, CT	V:Data Reg. V:Bit Reg. K:Constant	76 µs 158 µs 55 µs	12.0 µs 12.0 µs 12.0 µs
	1st	2nd		
	V: Data Reg.	V:Data Reg. V:Bit Reg. K:Constant	75 µs 158 µs 55 µs	12.0 µs 12.0 µs 12.0 µs
	V: Bit Reg.	V:Data Reg. V:Bit Reg. K:Constant	158 µs 240 µs 137 µs	12.0 µs 12.0 µs 12.0 µs
ANDN	1st	2nd		
	T, CT	V:Data Reg. V:Bit Reg. K:Constant	76 µs 158 µs 55 µs	12.0 µs 12.0 µs 12.0 µs
	1st	2nd		
	V: Data Reg.	V:Data Reg. V:Bit Reg. K:Constant	76 µs 158 µs 55 µs	12.0 µs 12.0 µs 12.0 µs
	V: Bit Reg.	V:Data Reg. V:Bit Reg. K:Constant	158 µs 240 µs 137 µs	12.0 µs 12.0 µs 12.0 µs

Immediate Instructions

Immediate Instructions		DL105	
Instruction	**Legal Data Types**	**Execute**	**Not Execute**
STRI	X	27 µs	9.8 µs
STRNI	X	26 µs	8.6 µs
ORI	X	27 µs	9.8 µs
ORNI	X	26 µs	8.6 µs
ANDI	X	25 µs	8.0 µs
ANDNI	X	24 µs	6.8 µs
OROUTI	Y	45 µs	45 µs
SETI	1st #: Y	25.5 µs	6.8 µs
	2nd #: Y (N pt)	5.5 µs+20 x N	6.8 µs
RSTI	1st #: Y	25.5 µs	6.8 µs
	2nd #: Y (N pt)	5 µs+20.5 x N	6.8 µs

Timer, Counter, Shift Register, EDRUM Instructions

Timer, Counter, Shift Register, and Drum Instructions			DL105	
Instruction	**Legal Data Types**		**Execute**	**Not Execute**
TMR	1st	2nd		
	T	V:Data Reg. V:Bit Reg. K:Constant	75 µs 158 µs 66 µs	31 µs 31 µs 31 µs
TMRF	1st	2nd		
	T	V:Data Reg. V:Bit Reg. K:Constant	75 µs 158 µs 66 µs	31 µs 31 µs 31 µs
TMRA	1st	2nd		
	T	V:Data Reg. V:Bit Reg. K:Constant	94 µs 304 µs 95 µs	56 µs 264 µs 45 µs
TMRAF	1st	2nd		
	T	V:Data Reg. V:Bit Reg. K:Constant	98 µs 304 µs 95 µs	54 µs 264 µs 49 µs
CNT	1st	2nd		
	CT	V:Data Reg. V:Bit Reg. K:Constant	68 µs 148 µs 56 µs	61 µs 141 µs 45 µs
SGCNT	1st	2nd		
	CT	V:Data Reg. V:Bit Reg. K:Constant	57 µs 140 µs 46 µs	64 µs 148 µs 53 µs

Timer, Counter, Shift Register, and Drum Instructions Cont'd		DL105	
Instruction	**Legal Data Types**	**Execute**	**Not Execute**
UDC	1st 2nd		
	CT V:Data Reg. V:Bit Reg. K:Constant	103 µs 310 µs 102 µs	74 µs 281 µs 70 µs
SR	C (N points to shift)	30 µs+4.6 µs xN	17.2 µs
EDRUM	CT	320 µs	221 µs

Accumulator Data Instructions

Accumulator / Stack Load and Output Data Instructions		DL105	
Instruction	**Legal Data Types**	**Execute**	**Not Execute**
LD	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	68 µs 149 µs 62 µs 169 µs 256 µs	8.4 µs 8.4 µs 8.4 µs 8.4 µs 8.4 µs
LDD	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	72 µs 266 µs 64 µs 172 µs 373 µs	8.4 µs 8.4 µs 8.4 µs 8.4 µs 8.4 µs
LDF	1st 2nd X, Y, C, S K:Constant T, CT, SP (N pt)	77 µs+6.2 µs xN	10 µs
LDA	O: (Octal constant for address)	58 µs	8.4 µs
OUT	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	60 µs 132 µs 162 µs 239 µs	8.4 µs 8.4 µs 8.4 µs 8.4 µs
OUTD	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	68 µs 276 µs 196 µs 384 µs	8.4 µs 8.4 µs 8.4 µs 8.4 µs
OUTF	1st 2nd X, Y, C K:Constant (N pt)	36 µs+7.6 µs xN	8 µs
POP	None	55 µs	7.2 µs

Logical Instructions

Logical (Accumulator) Instructions		DL105	
Instruction	**Legal Data Types**	**Execute**	**Not Execute**
AND	V:Data Reg. V:Bit Reg.	63 µs 261 µs	10.4 µs 10.4 µs
ANDD	K:Constant	53 µs	8.4 µs
OR	V:Data Reg. V:Bit Reg.	59 µs 257 µs	10.4 µs 10.4 µs
ORD	K:Constant	49 µs	8.4 µs
XOR	V:Data Reg. V:Bit Reg.	60 µs 257 µs	10.4 µs 10.4 µs
XORD	K:Constant	49 µs	8.4 µs
CMP	V:Data Reg. V:Bit Reg.	59 µs 259 µs	10.4 µs 10.4 µs
CMPD	V:Data Reg. V:Bit Reg. K:Constant	63 µs 257 µs 54 µs	8.4 µs 8.4 µs 8.4 µs

Math Instructions

Math Instructions (Accumulator)		DL105	
Instruction	**Legal Data Types**	**Execute**	**Not Execute**
ADD	V:Data Reg. V:Bit Reg.	198 µs 397 µs	10.6 µs 10.6 µs
ADDD	V:Data Reg. V:Bit Reg. K:Constant	198 µs 397 µs 188 µs	8.4 µs 8.4 µs 8.4 µs
SUB	V:Data Reg. V:Bit Reg.	200 µs 397 µs	10.6 µs 10.6 µs
SUBD	V:Data Reg. V:Bit Reg. K:Constant	198 µs 392 µs 190 µs	8.4 µs 8.4 µs 8.4 µs
MUL	V:Data Reg. V:Bit Reg. K:Constant	497 µs 483 µs 487 µs	10.6 µs 10.6 µs 8.4 µs
DIV	V:Data Reg. V:Bit Reg. K:Constant	909 µs 1108 µs 899 µs	10.6 µs 10.6 µs 8.4 µs
INCB	V:Data Reg. V:Bit Reg.	83 µs 349 µs	10.4 µs 10.4 µs
DECB	V:Data Reg. V:Bit Reg.	82 µs 351 µs	10.4 µs 10.4 µs

Bit Instructions

Bit Instructions (Accumulator)		DL105	
Instruction	**Legal Data Types**	**Execute**	**Not Execute**
SHFR	V:Data Reg. (N bits) V:Bit Reg. (N bits) K:Constant (N bits)	44μs+14.6 x N 243μs+14.6 x N 34μs+14.6 x N	10.4 μs 10.4 μs 8.4 μs
SHFL	V:Data Reg. (N bits) V:Bit Reg. (N bits) K:Constant (N bits)	44μs+14.6 x N 243μs+14.6 x N 34μs+14.6 x N	10.4 μs 10.4 μs 8.4 μs
ENCO	None	62 μs	7.2 μs
DECO	None	34 μs	7.2 μs

Number Conversion Instructions

Number Conversion Instructions (Accumulator)		DL105	
Instruction	**Legal Data Types**	**Execute**	**Not Execute**
BIN	None	359 μs	7.2 μs
BCD	None	403 μs	7.2 μs
INV	None	27 μs	5.0 μs

Table Instructions

Table Instructions		DL105	
Instruction	**Legal Data Types**	**Execute**	**Not Execute**
MOV	Move V:data reg. to V:data reg. Move V:bit reg. to V:data reg. Move V:data reg to V:bit reg. Move V:bit reg. to V:bit reg. N= #of words	450μs+17 x N 430μs+244 x N 460μs+215 x N 490μs+448 x N	6.2μs 6.2μs 6.2μs 6.2μs
MOVMC	Move V:Data Reg. to E^2 Move V:Bit Reg. to E^2 Move from E^2 to V:Data Reg. Move from E^2 to V:Bit Reg. N= #of words	— — 250μs+201xN —	— — 6.2μs —
LDLBL	K	58μs	8.4μs

CPU Control Instructions

CPU Control Instructions		DL105	
Instruction	**Legal Data Types**	**Execute**	**Not Execute**
NOP	None	0 µs	0 µs
END	None	27 µs	27 µs
STOP	None	16 µs	5 µs

Program Control Instructions

Program Control Instructions		DL105	
Instruction	**Legal Data Types**	**Execute**	**Not Execute**
MLS	K (1-7)	12 µs	12 µs
MLR	K (0-6) N= 1 to 7	13 µs + 2.4 x N	13 µs + 2.4 x N

Interrupt Instructions

Interrupt Instructions		DL105	
Instruction	**Legal Data Types**	**Execute**	**Not Execute**
ENI	None	9 µs	5 µs
DISI	None	8 µs	5 µs
INT	O0	0 µs	0 µs
IRT	None	1.6 µs	—

Message Instructions

Message Instructions		DL105	
Instruction	**Legal Data Types**	**Execute**	**Not Execute**
FAULT	V:Data Reg. V:Bit Reg. K:Constant	171 µs 253 µs 2798 µs	8.4 µs 8.4 µs 8.4 µs
DLBL	K	0 µs	0 µs
NCON	K	0 µs	0 µs
ACON	K	0 µs	0 µs

RLL*PLUS* Instructions

RLL*PLUS* Instructions		DL105	
Instruction	**Legal Data Types**	**Execute**	**Not Execute**
ISG	S	31 µs	32 µs
SG	S	31 µs	32 µs
JMP	S	14 µs	8 µs