C

Appendix C Determining I/O Update Time

— Overview
— Calculating Input Signal Delay Time
— Calculating Output Signal Delay Time
— Calculating Total System Delay Time

Overview

Since the Slice Master and the CPU operate asynchronously from one another, it is possible that the remote I/O points may not be updated on every CPU scan. Therefore, if you have I/O points that must be updated on every scan, you should place them in the local and/or expansion base. In some applications it may helpful to understand the amount of time required to update the Slice I/O points. Depending on the number of I/O points used in your Slice configuration and the baud rate you have selected for communication, your update time requirements will vary. This Appendix will show you how to estimate the total delay time for your system.

NOTE: In most situations, this delay will be so small that either it makes no difference to the particular application or the mechanical speeds of the field devices are slower than the delay itself.

If you have an application that requires a thorough understanding of the time delay, you can use the following information in order to calculate the delay:

- **Baud Rate —** this is the communication baud rate that you selected with the dipswitch settings on the slice master and slice slaves.
- **CPU Scan Time —** this is the total CPU scan time. The easiest way is to use AUX53 from a DL405 Handheld Programmer, or use the Diagnostics option under the PLC menu in our ***Direct***SOFT Programming Software. You can also use the DL405 User Manual to calculate the scan time, but this is often very time consuming. If you use the User Manual, you will have to estimate this time, because it is dependent on the main program length, and number of I/O points in the local and expansion bases as well.
- **Slice Master Scan —** this is the time required for the Slice Master to scan the individual Slave stations to update the status of the I/O modules. Use the formula and table shown on the following page.
- **Module ON to OFF, OFF to ON Response Time —** this is the amount of time that the module requires to see a transition in status. For example, when a switch connected to an input module closes, it can take a few milliseconds (1–12 typical) before the module actually makes the transition from OFF to ON. Check the detailed specifications in Chapter 1 for the Slice slave response times. This basic information is also available in the specifications of the Sales Catalog.
- **Total Delay Time —** this is the total delay time that takes all of the above factors into consideration. There are several formulas that can be used to calculate this delay time. The pages that follow will show you those formulas. Once you have selected the applicable formula, you will use the information you have gathered for the above items to calculate the total system delay time.

Since each application is different, we cannot possibly show all of the options for the CPU scan time or the possible module response delays. You can easily find this information in other publications. However, the next few pages *will* show you how to calculate the delay time for the Slice Master Scan. Also, we show the total delay time for our example system that was used earlier in this manual.

Calculating Input Signal Delay Time

Input Delay Time Formulas

The formulas shown below show you how much time is required for the CPU to detect an OFF-to-ON transition for an input switch at the slave station.

- Minimum Delay: I_{min} = F+910 μs
- Maximum Delay: I_{max} = F+2B +C

F = Time delay for input filter(s)
ON to OFF = 12 ms (maximum)
OFF to ON = 7 ms (maximum)
B = Bus scan time (See table below.)
C = CPU scan time (With ***Direct***SOFT, click on PLC/Diagnostics/Scan Time)
As an alternative, use AUX53 of the handheld programmer to find this out.

Slot Location of the Master	V-memory Location where the bus scan time is calculated and stored as a hexadecimal number of milliseconds
0	V7710
1	V7711
2	V7712
3	V7713
4	V7714
5	V7715
6	V7716
7	V7717

Example for Computing Input Delay

In this example, we are examining the OFF to ON transition for the input delay of a slave belonging to a master that is located in Slot 2 of the CPU base.

1. Use the maximum delay formula: I_{max} = F+2B +C
2. Use 7ms maximum filter delay time.
3. Place the CPU in RUN mode.
4. Use the table above to find the memory location that contains the bus scan time. For example, let's say it is 12ms.
5. Use ***Direct***SOFT or AUX 53 from a handheld programmer to determine the CPU scan time. For illustration, let's say you discover it is 20 ms.
6. Solve the equation from Step 1:
   I_{max} = F + 2B +C
   I_{max} = 7 + 2(12) +20
   I_{max} = 51ms

Calculating Output Signal Delay Time

Output Delay Time Formulas

Here we are measuring the amount of time it takes for the CPU to turn ON an output at the Slice Slave. The formulas for computing this are as follows:

- OUT_{min} = 1.12 ms
- OUT_{max} = 0.5 ms + 2B +C

OUT_{min} = Minimum output signal delay
OUT_{max} =Maximum output signal delay
0.5 ms = Output hardware response time
B =Bus scan time (See Table Below.)
C = CPU scan time (follow instructions on Page C-3)

Slot Location of the Master	V-memory Location where the bus scan time is calculated and stored as a hexadecimal number of milliseconds
0	V7710
1	V7711
2	V7712
3	V7713
4	V7714
5	V7715
6	V7716
7	V7717

Example for Computing Output Delay

In this example, we are examining the maximum time an output point is delayed when transitioning from OFF to ON. Here we are measuring an output point on a slave belonging to a master located in Slot 4.

1. Use the maximum delay formula: OUT_{max} = 0.5ms + 2B +C
2. Place the CPU in the RUN mode.
3. Use the table to find where to check in memory for the bus scan time. For illustration, let's say you discover it is 15 ms.
4. Use ***Direct***SOFT or AUX53 of the handheld programmer to determine the CPU scan time. For illustration, let's say you discover it is 12 ms.
5. Solve the equation from Step 1:
   OUT_{max} = 0.5 ms + 2B + C
   OUT_{max} = 0.5 ms + 2(15) + 12
   OUT_{max} = 42.5 ms

Calculating Total System Delay Time

Output Delay Time Formulas

Here we are calculating the total delay time for a simple Slice I/O example. Once the Slice slave input comes on, we want to know how long it will take the system to sense the input change, transfer the data back to the CPU, and then update the Slice slave output point.The formulas for computing this are as follows:

- $TOT_{min} = I_{min} + B + C$
- $TOT_{max} = I_{max} + 4B + C$
- $TOT_{avg} = I_{min} + 2B + C$

TOT_{min} = Minimum total signal delay
TOT_{max} = Maximum total signal delay
TOT_{avg} = Average total signal delay
I_{max} = Maximum input signal delay
I_{min} = Minimum input signal delay
B =Bus scan time (See Table Below.)
C = CPU scan time (follow instructions on Page C-3)

Slot Location of the Master	V-memory Location where the bus scan time is calculated and stored as a hexadecimal number of milliseconds
0	V7710
1	V7711
2	V7712
3	V7713
4	V7714
5	V7715
6	V7716
7	V7717

Table Showing Approximate Signal Delay Times

Before you actually do your own computations using the formulas above, you may want to have an approximate idea of how much total delay time you should expect. This table should provide that information. We leave the actual computation up to you. In this example, we are assuming that we are using a 440 CPU and the scan time for a hypothetical example program is 20 ms (Use ***Direct***SOFT or AUX53 to find the time for your program). We are also assuming a baud rate of153.6 kB between the Slice Master and the Slice Slaves.

# of Remotes	TOTmin (ms)	TOTavg (ms)	Tmax (ms)
2	30.7	34.3	41.6
4	34.2	41.4	55.8
6	37.8	48.5	70.0
8	41.3	55.6	84.2
10	44.8	62.7	92.7
12	48.4	69.7	112.4