C

Instruction Execution Times

In This Appendix. . . .

Introduction

This appendix contains several tables that provide the instruction execution times for the DL350 CPU. You will notice is that many of the execution times depend on the type of data being used with the instruction. For example, a few of the instructions that use V-memory locations are further defined by the following items.

- Data Registers
- Bit Registers

V-Memory Data Registers

Some V-memory locations are considered data registers. For example, the V-memory locations that store the timer or counter current values, or just regular user V–memory would be considered as a V-memory data register. Don't think that you cannot load a bit pattern into these types of registers, you can. It's just that their primary use is as a data register. The following locations are considered as data registers.

Data Registers	DL350
Timer Current Values	V0 – V377
Counter Current Values	V1000 – V1177
User Data Words	V1400 – V7377 V10000 – V17777

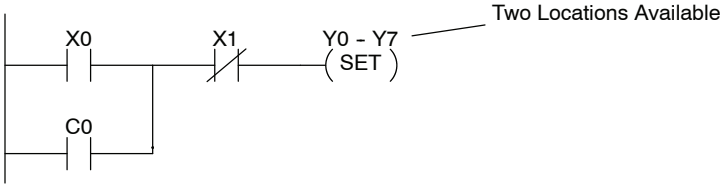
V-Memory Bit Registers

You may recall that some of the discrete points such as X, Y, C, etc. are automatically mapped into V–memory. The following locations that contain this data are considered bit registers.

Bit Registers	DL350
Input Points (X)	V40400 – V 40437
Output Points (Y)	V40500 – V40537
Control Relays (C)	V40600 – V40677
Timer Status Bits	V41100 – V41117
Counter Status Bits	V41040 – V41147
Stages	V41000 – V41077

How to Read the Tables

Some of the instructions can have more than one parameter so the table shows execution times that depend on the amount and type of parameters. For example, the SET instruction can be used to set a single point or a range of points. If you examine the execution table you'll notice the available data types and execution times for both situations. The following diagram shows an example.



Execution depends on numbers of locations and types of data used

SET	1st #:	X, Y, C, S	17.4 µs
	2nd #:	X, Y, C, S, (N pt)	12.0µs+5.4µsxN
RST	1st #:	X, Y, C, S	19.5 µs
	2nd #:	X, Y, C, S, (N pt)	10.5µs+5.2µsxN

Boolean Instructions

Boolean Instructions		DL350	
Instruction	**Legal Data Types**	**Execute**	**Not Exec**
STR	X, Y, C, T, CT,S, SP	.74 µs	.74 µs
STRN	X, Y, C, T, CT,S, SP	0.68 µs	0.74 µs
OR	X, Y, C, T, CT, S, SP	0.56 µs	0.56 µs
ORN	X, Y, C, T, CT,S, SP	0.6 µs	0.6 µs
AND	X, Y, C, T, CT, S, SP	0.46 µs	0.46 µs
ANDN	X, Y, C, T, CT, S, SP	0.56 µs	0.56 µs
ANDSTR	None	0.4 µs	0.4 µs
ORSTR	None	0.4 µs	0.4 µs
OUT	X, Y, C	2.0 µs	2.0 µs
OUTH	X, Y, C	1.1 µs	1.1 µs
OROUT	X, Y, C	2.4 µs	2.4 µs
PD	X, Y, C	16.6 µs	16.6 µs
SET	1st #: X, Y, C, S 2nd #: X, Y, C, S (N pt)	10.6 µs 11.4µs+ 0.9µsxN	1.1 µs 1.1 µs
RST	1st #: X, Y, C, S 2nd #: X, Y, C, S (N pt)	10.6 µs 11.4µs+ 0.9µsxN	1.1 µs 1.1 µs
	1st #: T, CT 2nd #: T, CT (N pt)	10.6 µs 11.4µs+ 0.9µsxN	1.1 µs 1.1 µs

Comparative Boolean

Comparative Boolean Instructions			DL350	
Instruction	**Legal Data Types**		**Execute**	**Not Exec**
STRE	1st	2nd		
	V: Data Reg.	V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.		
		K:Constant	5.5µs	5.5µs
		P:Indir. (Data)	35.9µs	35.9µs
		P:Indir. (Bit)		
	V: Bit Reg.	V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.		
		K:Constant	5.5µs	5.5µs
		P:Indir. (Data)	35.9µs	35.9µs
		P:Indir. (Bit)		
	P:Indir. (Data)	V:Data Reg.	—	
		V:Bit Reg.	35.6µs	35.6µs
		K:Constant		
		P:Indir. (Data)	32.6µs	32.6µs
		P:Indir. (Bit)	60.7µs	60.7µs
	P:Indir. (Bit)	V:Data Reg.		
		V:Bit Reg.	35.6µs	35.6µs
		K:Constant		—
		P:Indir. (Data)	32.6µs	32.6µs
		P:Indir. (Bit)	60.7µs	60.7µs
STRNE	1st	2nd		
	V: Data Reg.	V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.		
		K:Constant	5.5µs	5.5µs
		P:Indir. (Data)	35.9µs	35.9µs
		P:Indir. (Bit)		
	V: Bit Reg.	V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.		
		K:Constant	5.5µs	5.5µs
		P:Indir. (Data)	35.9µs	35.9µs
		P:Indir. (Bit)		
	P:Indir. (Data)	V:Data Reg.	—	—
		V:Bit Reg.	35.6µs	35.6µs
		K:Constant		
		P:Indir. (Data)	32.6µs	32.6µs
		P:Indir. (Bit)	60.7µs	60.7µs
	P:Indir. (Bit)	V:Data Reg.	35.6µs	35.6µs
		V:Bit Reg.		
		K:Constant	32.6µs	32.6µs
		P:Indir. (Data)	60.7µs	60.7µs
		P:Indir. (Bit)		

Comparative Boolean (cont.)			DL350	
Instruct	**Legal Data Types**		**Execute**	**Not Exec**
ORE	1st	2nd		
	V: Data Reg.	V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.		
		K:Constant	5.5µs	5.5µs
		P:Indir. (Data)	35.9µs	35.9µs
		P:Indir. (Bit)		
	V: Bit Reg.	V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.		
		K:Constant	5.5µs	5.5µs
		P:Indir. (Data)	35.9µs	35.9µs
		P:Indir. (Bit)		
	P:Indir. (Data)	V:Data Reg.	—	—
		V:Bit Reg.	35.6µs	35.6µs
		K:Constant	32.6µs	32.6µs
		P:Indir. (Data)	60.7µs	60.7µs
		P:Indir. (Bit)		
	P:Indir. (Bit)	V:Data Reg.	35.6µs	35.6µs
		V:Bit Reg.		
		K:Constant	32.6µs	32.6µs
		P:Indir. (Data)	60.7µs	60.7µs
		P:Indir. (Bit)		
ORNE	1st	2nd		
	V: Data Reg.	V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.		
		K:Constant	5.5µs	5.5µs
		P:Indir. (Data)	35.9µs	35.9µs
		P:Indir. (Bit)		
	V: Bit Reg.	V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.		
		K:Constant	5.5µs	5.5µs
		P:Indir. (Data)	35.9µs	35.9µs
		P:Indir. (Bit)		
	P:Indir. (Data)	V:Data Reg.	—	—
		V:Bit Reg.	35.6µs	35.6µs
		K:Constant	32.6µs	32.6µs
		P:Indir. (Data)	60.7µs	60.7µs
		P:Indir. (Bit)		
	P:Indir. (Bit)	V:Data Reg.	35.6µs	35.6µs
		V:Bit Reg.		
		K:Constant	32.6µs	32.6µs
		P:Indir. (Data)	60.7µs	60.7µs
		P:Indir. (Bit)		

Comparative Boolean (cont.)			DL350	
Instruct	**Legal Data Types**		**Execute**	**Not Exec**
ANDE	1st	2nd		
	V: Data Reg.	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	8.7µs 5.5µs 35.9µs 	8.7µs 5.5µs 35.9µs
	V: Bit Reg.	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	8.7µs 5.5µs 35.9µs —	8.7µs 5.5µs 35.9µs —
	P:Indir. (Data)	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	35.6µs 32.6µs 60.7µs 	35.6µs 32.6µs 60.7µs
	P:Indir. (Bit)	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	35.6µs 32.6µs 60.7µs 	35.6µs 32.6µs 60.7µs
ANDNE	1st	2nd		
	V: Data Reg.	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	8.7µs 5.5µs 35.9µs 	8.7µs 5.5µs 35.9µs
	V: Bit Reg.	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	8.7µs 5.5µs 35.9µs —	8.7µs 5.5µs 35.9µs —
	P:Indir. (Data)	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	35.6µs 32.6µs 60.7µs 35.6µs	35.6µs 32.6µs 60.7µs 35.6µs
	P:Indir. (Bit)	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	 32.6µs 60.7µs 	 32.6µs 60.7µs

Comparative Boolean (cont.)			DL350	
Instruc	**Legal Data Types**		**Execute**	**Not Exec**
STR	1st	2nd		
	T, CT	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	8.7µs 5.5µs 35.9µs	8.7µs 5.5µs 35.9µs
	1st	2nd		
	V: Data Reg.	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	8.7µs 5.5µs 35.9µs	8.7µs 5.5µs 35.9µs
	V: Bit Reg.	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	8.7µs 5.5µs 35.9µs	8.7µs 5.5µs 35.9µs
	P:Indir. (Data)	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	— 35.6µs 32.6µs 60.7µs	— 35.6µs 32.6µs 60.7µs
	P:Indir. (Bit)	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	35.6µs 32.6µs 60.7µs	35.6µs 32.6µs 60.7µs
STRN	1st	2nd		
	T, CT	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	8.7µs 5.5µs 35.9µs	8.7µs 5.5µs 35.9µs
	1st	2nd		
	V: Data Reg.	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	8.7µs 5.5µs 35.9µs	8.7µs 5.5µs 35.9µs
	V: Bit Reg.	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	8.7µs 5.5µs 35.9µs	8.7µs 5.5µs 35.9µs
	P:Indir. (Data)	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	— 35.6µs 32.6µs 60.7µs	— 35.6µs 32.6µs 60.7µs
	P:Indir. (Bit)	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	35.6µs 32.6µs 60.7µs	35.6µs 32.6µs 60.7µs

Comparative Boolean (cont.)			DL350	
Instruc	**Legal Data Types**		**Execute**	**Not Exec**
OR	1st	2nd		
	T, CT	V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.		
		K:Constant	5.5µs	5.5µs
		P:Indir. (Data)	35.9µs	35.9µs
		P:Indir. (Bit)		
	1st	2nd		
	V: Data Reg.	V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.		
		K:Constant	5.5µs	5.5µs
		P:Indir. (Data)	35.9µs	35.9µs
		P:Indir. (Bit)		
	V: Bit Reg.	V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.		
		K:Constant	5.5µs	5.5µs
		P:Indir. (Data)	35.9µs	35.9µs
		P:Indir. (Bit)		
	P:Indir. (Data)	V:Data Reg.	—	—
		V:Bit Reg.	35.6µs	35.6µs
		K:Constant		
		P:Indir. (Data)	32.6µs	32.6µs
		P:Indir. (Bit)	60.7µs	60.7µs
	P:Indir. (Bit)	V:Data Reg.	35.6µs	35.6µs
		V:Bit Reg.		
		K:Constant	32.6µs	32.6µs
		P:Indir. (Data)	60.7µs	60.7µs
		P:Indir. (Bit)		
ORN	1st	2nd		
	T, CT	V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.		
		K:Constant	5.5µs	5.5µs
		P:Indir. (Data)	35.9µs	35.9µs
		P:Indir. (Bit)		
	1st	2nd		
	V: Data Reg.	V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.		
		K:Constant	5.5µs	5.5µs
		P:Indir. (Data)	35.9µs	35.9µs
		P:Indir. (Bit)		
	V: Bit Reg.	V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.		
		K:Constant	5.5µs	5.5µs
		P:Indir. (Data)	35.9µs	35.9µs
		P:Indir. (Bit)		
	P:Indir. (Data)	V:Data Reg.	—	—
		V:Bit Reg.	35.6µs	35.6µs
		K:Constant		
		P:Indir. (Data)	32.6µs	32.6µs
		P:Indir. (Bit)	60.7µs	60.7µs
	P:Indir. (Bit)	V:Data Reg.	35.6µs	35.6µs
		V:Bit Reg.		
		K:Constant	32.6µs	32.6µs
		P:Indir. (Data)	60.7µs	60.7µs
		P:Indir. (Bit)		

Comparative Boolean (cont.)			DL350	
Instruc	**Legal Data Types**		**Execute**	**Not Exec**
AND	1st	2nd		
	T, CT	V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.		
		K:Constant	5.5µs	5.5µs
		P:Indir. (Data)	35.9µs	35.9µs
		P:Indir. (Bit)		
	1st	2nd		
	V: Data Reg.	V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.		
		K:Constant	5.5µs	5.5µs
		P:Indir. (Data)	35.9µs	35.9µs
		P:Indir. (Bit)		
	V: Bit Reg.	V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.		
		K:Constant	5.5µs	5.5µs
		P:Indir. (Data)	35.9µs	35.9µs
		P:Indir. (Bit)		
	P:Indir. (Data)	V:Data Reg.	—	—
		V:Bit Reg.	35.6µs	35.6µs
		K:Constant	32.6µs	32.6µs
		P:Indir. (Data)	60.7µs	60.7µs
		P:Indir. (Bit)		
	P:Indir. (Bit)	V:Data Reg.	35.6µs	35.6µs
		V:Bit Reg.		
		K:Constant	32.6µs	32.6µs
		P:Indir. (Data)	60.7µs	60.7µs
		P:Indir. (Bit)		
ANDN	1st	2nd		
	T, CT	V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.		
		K:Constant	5.5µs	5.5µs
		P:Indir. (Data)	35.9µs	35.9µs
		P:Indir. (Bit)		
	1st	2nd		
	V: Data Reg.	V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.		
		K:Constant	5.5µs	5.5µs
		P:Indir. (Data)	35.9µs	35.9µs
		P:Indir. (Bit)		
	V: Bit Reg.	V:Data Reg.	8.7µs	8.7µs
		V:Bit Reg.		
		K:Constant	5.5µs	5.5µs
		P:Indir. (Data)	35.9µs	35.9µs
		P:Indir. (Bit)		
	P:Indir. (Data)	V:Data Reg.	—	—
		V:Bit Reg.	35.6µs	35.6µs
		K:Constant	32.6µs	32.6µs
		P:Indir. (Data)	60.7µs	60.7µs
		P:Indir. (Bit)		
	P:Indir. (Bit)	V:Data Reg.	35.6µs	35.6µs
		V:Bit Reg.		
		K:Constant	32.6µs	32.6µs
		P:Indir. (Data)	60.7µs	60.7µs
		P:Indir. (Bit)		

Immediate Instructions

Immediate Instructions		DL350	
Instruc	**Legal Data Types**	**Execute**	**Not Exec**
STRI	X	78.6 µs	78.6 µs
STRNI	X	78.6 µs	78.6 µs
ORI	X	78.6 µs	78.6 µs
ORNI	X	78.6 µs	78.6 µs
ANDI	X	78.6 µs	78.6 µs
ANDNI	X	78.6 µs	78.6 µs
OUTI	Y	91.0 µs	91.0 µs
OROUTI	Y	94.0 µs	94.0 µs
SETI	1st #: Y 2nd #: Y (N pt)	87.6 µs 97.5µs+ 16.25xN	1.1 µs 1.1 µs
RSTI	1st #: Y 2nd #: Y (N pt)	87.6 µs 97.5µs+ 16.25xN	1.1 µs

Timer, Counter, Shift Register Instructions

Timer, Counter, Shift Register Instructions			DL350	
Instruc	**Legal Data Types**		**Execute**	**Not Exec**
TMR	1st	2nd		
	T	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	38.6µs 23.0µs 54.3µs	24.6µs 24.6µs 52.0µs
TMRF	1st	2nd		
	T	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	61.2µs 57.6µs 90.4µs	23.0µs 19.4µs 37.5µs
TMRA	1st	2nd		
	T	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	58.2µs 53.6µs 90.4µs	27.1µs 22.4µs 59.2µs
TMRAF	1st	2nd		
	T	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	64.5µs 59.9µs 96.7µs	27.6µs 22.4µs 59.2µs
CNT	1st	2nd		
	CT	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	36.1µs 32.5µs 97.1µs	24.6µs 21.0µs 56.8µs
SGCNT	1st	2nd		
	CT	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	35.2µs 33.7µs 67.4µs	27.7µs 27.1µs 57.9µs
UDC	1st	2nd		
	CT	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	47.4µs 42.7µs 81.7µs	40.0µs 35.3µs 72.1µs
SR	C (N points to shift)		17.8µs+ 1.0µsxN	12.6 µs

Accumulator Data Instructions

Accumulator / Stack Load and Output Data Instructions		DL350	
Instruc	**Legal Data Types**	**Execute**	**Not Exec**
LD	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	13.6µs 10.4µs 40.4µs	1.1µs 1.1µs 1.1µs
LDD	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	14.0µs 10.4µs 45.0µs	1.1µs 1.1µs 1.3µs
LDF	1st: X, Y, C, S, T, CT, SP 2nd: K:Constant	10.5µs+ 3.45µs x N	1.4µs
LDA	O: (Octal constant for address)	10.4 µs	1.1µs
LDSX	K: Constant	14.6 µs	1.5µs
OUT	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	10.7 µs 41.9 µs	1.1µs
OUTD	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	11.7 µs 42.6 µs	1.1µs
OUTF	1st: X, Y, C 2nd: K:Constant	43.8µs+ 6.2µs x N	1.1µs
POP	None	7.8 µs	1.0µs

Logical Instructions

Logical (Accumulator) Instructions		DL350	
Instruc	**Legal Data Types**	**Execute**	**Not Exec**
AND	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	9.1µs 39.8µs	1.1µs 1.1µs
ANDD	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	10.2µs 6.5µs 40.9µs	1.1µs 1.1µs 1.1µs
OR	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	9.3µs 40.2µs	1.1µs 1.1µs
ORD	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	10.4µs 6.7µs 41.1µs	1.1µs 1.1µs 1.1µs
XOR	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	9.2µs 40.0µs	1.1µs 1.1µs
XORD	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	10.3µs 6.2µs 41.0µs	1.1µs 1.1µs 1.1µs
CMP	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	10.8µs 41.5µs	1.1µs 1.1µs
CMPD	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	11.4µs 7.7µs 42.1µs	1.2µs 1.2µs 1.2µs
CMPS	None	—	—

Math Instructions

Math Instructions (Accumulator)		DL350	
Instruc	**Legal Data Types**	**Execute**	**Not Exec**
ADD	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	93.3µs 129.8µs	1.2µs 1.1µs
ADDD	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	99.2µs 80.6µs 129.8µs	1.2µs 1.2µs 1.2µs
SUB	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	92.1µs 121.9µs	1.1µs 1.1µs
SUBD	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	98.2µs 78.6µs 127.8µs	1.1µs 1.1µs 1.1µs
MUL	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	341.1µs 367.8 371.8µs	1.1µs 1.1µs 1.1µs
MULD	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	1075.8µs 1106.5µs	1.1µs 1.1µs
DIV	V:Data Reg. V:Bit Reg. K:Constant P:Indir. (Data) P:Indir. (Bit)	466.6µs 492.8µs 538.2µs	1.1µs 1.1µs 1.1µs
DIVD	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	510.6µs 501.1µs	1.1µs 1.1µs
INCB	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	15.2µs 45.9µs	1.1µs 1.1µs
DECB	V:Data Reg. V:Bit Reg. P:Indir. (Data) P:Indir. (Bit)	15.2µs 45.2µs	1.1µs 1.1µs

Bit Instructions

Bit Instructions (Accumulator)		DL350	
Instruc	**Legal Data Types**	**Execute**	**Not Exec**
SHFR	V:Data Reg. (N bits) V:Bit Reg. (N bits) K:Constant (N bits)	9.8µs+ 0.2 x N 7.9µs+0.2 x N	1.2 µs
SHFL	V:Data Reg. (N bits) V:Bit Reg. (N bits) K:Constant (N bits)	9.8µs+ 0.2 x N 7.9µs+ 0.2 x N	1.2 µs
ROTR	V:Data Reg. (N bits) V:Bit Reg. (N bits) K:Constant (N bits)	15.7 12.3	1.2 µs
ROTL	V:Data Reg. (N bits) V:Bit Reg. (N bits) K:Constant (N bits)	15.7µs 12.3µs	1.2 µs
ENCO	None	40.3 µs	1.0 µs
DECO	None	6.5 µs	1.0 µs

Number Conversion Instructions

Number Conversion Instructions (Accumulator)		DL350	
Instruc	**Legal Data Types**	**Execute**	**Not Exec**
BIN	None	128.4 µs	1.0 µs
BCD	None	122.0 µs	1.0 µs
INV	None	2.9 µs	1.0 µs
BCDCPL	None	74.5 µs	1.0 µs
ATH	None	29.2 µs	1.0 µs
HTA	None	29.2 µs	1.0 µs
SEG	None	12.6 µs	1.0 µs
GRAY	None	142.0 µs	1.0 µs
SFLDGT	None	26.6 µs	1.0 µs

Table Instructions

Table Instructions		DL350	
Instruc	**Legal Data Types**	**Execute**	**Not Exec**
MOV	Move V:data reg. to V:data reg . Move V:bit reg. to V:data reg. Move V:data reg to V:bit reg. Move V:bit reg. to V:bit reg. N= #of words	63µs+ 16xN	1.20 µs
MOVMC	Move V:Data Reg. to E^2 Move V:Bit Reg. to E^2 Move from E^2 to V:Data Reg. Move from E^2 to V:Bit Reg. N= #of words	50µs+ 15xN	1.2 µs
LDLBL	K	7.4µs	1.5 µs

CPU Control Instructions

CPU Control Instructions		DL350	
Instruct	**Legal Data Types**	**Execute**	**Not Exec**
NOP	None	0.6 µs	0.6 µs
END	None	14.7 µs	14.7 µs
STOP	None	4.1 µs	1.0 µs
RSTWT	None	5.4 µs	1.0 µs
NOT	None	1.0 µs	1.0 µs

Program Control Instructions

Program Control Instructions		DL350	
Instruct	**Legal Data Types**	**Execute**	**Not Exec**
GOTO	K	5.0 µs	4.9 µs
LBL	K	0.6 µs	0.6 µs
FOR	V, K	110 µs	7.9 µs
NEXT	None	48.4 µs	0 µs
GTS	K	12.5 µs	6.3 µs
SBR	K	0.5 µs	0 µs
RT	None	11.4 µs	11.4 µs
MLS	K (1–7)	4.2 µs	4.2 µs
MLR	K (0–7)	4.0 µs	4.0 µs

Interrupt Instructions

Interrupt Instructions		DL350	
Instruc	**Legal Data Types**	**Execute**	**Not Exec**
ENI	None	45.8 µs	1.1 µs
DISI	None	5.7 µs	1.1 µs
INT	0 (0–7)	0 µs	0 µs
IRT	None	1.5 µs	—
IRTC	None	0.5 µs	0.5

Network Instructions

Network Instructions		DL350	
Instruc	**Legal Data Types**	**Execute**	**Not Exec**
RX	X, Y, C, T, CT, SP, S V:Data Reg. V:Bit Reg.	2024.1 µs	1.4 µs
WX	X, Y, C, T, CT, SP, S V:Data Reg. V:Bit Reg.	2024.1 µs	1.4 µs

Message Instructions

Message Instructions		DL350	
Instruc	**Legal Data Types**	**Execute**	**Not Exec**
FAULT	V:Data Reg. V:Bit Reg. K:Constant	108.9 µs 108.9 µs 96.2 µs	1.4 µs 1.4 µs 1.4 µs
DLBL	K	0 µs	0 µs
NCON	K	0 µs	µs
ACON	K	0 µs	0 µs
PRINT		104.0 µs	1.4 µs

RLL*PLUS* Instructions

RLL*PLUS* Instructions		DL350	
Instruc	**Legal Data Types**	**Execute**	**Not Exec**
ISG	S	24.3 µs	21.5 µs
SG	S	24.3 µs	21.5 µs
JMP	S	24.4 µs	4.3 µs
NJMP	S	24.4 µs	4.6 µs
CV	S	13.9 µs	13.9 µs
CVJMP	S (N stages, 1 to 16)	12.6µs	12.6 µs
BCALL	C	17.1 µs	17.1 µs
BLK	C	22.1 µs	22.6 µs
BEND	None	8.7 µs	0 µs

Clock / Calendar Instructions

Clock / Calendar Instructions		DL350	
Instruction	**Legal Data Types**	**Execute**	**Not Exec**
DATE	V:Data Reg. V:Bit Reg.	21.3 µs 21.3 µs	1.9 µs 1.9 µs
TIME	V:Data Reg. V:Bit Reg.	13.2 µs 13.2 µs	1.9 µs 1.9 µs

Drum Instructions

Drum Instructions		DL350	
Instruction	**Legal Data Types**	**Execute**	**Not Exe.**
DRUM	CT	340.0 µs	62.6 µs
EDRUM	CT	243.0 µs	100.0 µs
MDRMD	CT	206.0 µs	142.00 µs
MDRMW	CT	150.0 µs	94.00 µs